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Ultrathin Catalytic Condensers with engineered Pt/HfO_2 interfaces for charge modulation

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Abstract. Catalytic condensers offer a flexible platform for programmable catalysis by modulating the electronic properties of active sites through applied voltage. Constructed as metal-oxide-semiconductor (MOS) stacks, these devices feature a high-k dielectric separating two conductive films, with the top electrode serving as both a catalytic layer and charge distributor. Here, we enhanced the architecture of the catalytic condensers to improve charge distribution and localization. By reducing the hafnia dielectric thickness from 70 nm to sub-5 nm using an optimized Atomic Layer Deposition (ALD) process and integrating single-layer graphene as a charge distributor, we achieved a charge density of 4.6 x 10^{13} charges cm^{-2} without exceeding a leak current of 100 µA cm^{-2}. Systematic ALD studies revealed that purge time affects the dielectric constant and resulting leak current, enabling the fabrication of a more electrically insulating and thin dielectric layer. These optimized condensers demonstrated leak currents as low as 1 nA cm^{-2} at 1.0 x 10^{13} charges cm^{-2}. The ultrathin catalytic condensers were then used to explore several new geometries aimed at maximizing charge accumulation per platinum atom. The most effective design, the "blanket condenser," featured small platinum nanoislands at the interface of the top electrode and hafnia dielectric, covered by either single-layer graphene or porous carbon nanotubes. This configuration effectively blanketed the nanoislands, closing the electrical circuit while minimizing the distance between the dielectric and the active nanoislands. Compared to a continuous platinum electrode, the blanket condenser enabled accumulation of significantly more charge per platinum atom, opening new opportunities for catalytic applications.

Introduction. Modulating the electronic properties of heterogeneous catalysts is a powerful handle used to influence catalytic activity and selectivity.[1–3] Traditional methods have relied on altering synthesis conditions or support materials to achieve the desired electronic effects on the active site. However, these approaches suffer from limitations, including the inability to adjust electronic states during catalytic cycles. Catalytic condensers have emerged as a promising solution to dynamically modulate charge at the catalyst-support interface during reactions.[4,5]

Catalytic condensers function as metal-oxide-semiconductor (MOS) capacitors where a thin (< 10 nm) metal electrode also serves as the catalytic surface.[6,7] By adjusting the applied voltage between the doped semiconductor and metal electrodes, the quantity of electrons or holes stored in the catalytic layer can be precisely controlled. This level of control provides access to unique electronic states in the catalyst and allows for dynamic modulation of these states during reactions.[8,9]

The degree of charge modulation in catalytic condensers depends on the total charge condensed, Q, which is the product of the device capacitance, C, and the applied voltage, V (i.e., $Q = CV$). In the pioneering work by Onn et al., catalytic condensers with a 70 nm-thick hafnia dielectric were fabricated, achieving capacitances ranging from 280 to 350 nF cm^{-2}.[6,7] These devices featured a conductive catalyst layer composed of single-layer graphene (SLG) with platinum or amorphous alumina (2-10 nm) deposited on top. SLG is an ideal charge distributor due to its high electrical conductivity and atomic thickness.[10] Notably, devices without the catalyst layer exhibited a tenfold decrease in capacitance, suggesting a significant portion of the charge was stored within this layer. However, this decrease in capacitance could also result from differences between actual and measured graphene areas due to challenges in the graphene transfer process. It is thus plausible that in the presence of the catalytic layer, the thin platinum film reconnects any isolated islands of graphene, enhancing the measured capacitance.

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In subsequent catalytic condenser work, the difficulties of working with graphene were circumvented by replacing the graphene layer with an amorphous sputter-coated carbon layer (1-10 nm).[11] This modification allowed for the scalable manufacturing of catalytic condensers from 1 cm^2 up to 42 cm^2, achieving a room temperature capacitance of 195 nF cm^{-2}. Further improvements were pursued by investigating alternative dielectric materials to improve both capacitance and breakdown voltage—the maximum voltage before device failure under a strong electric field. For example, Oh et al. increased capacitance to 1200 nF cm^{-2} at room temperature using alternating nanolaminate layers of alumina (Al_2O_3) and titania (TiO_2), though this approach suffered from relatively high leak currents (~1 μA at 1V).[12] Leakage current is the undesired flow of current through the dielectric, leading to energy losses in catalytic condensers. Onn et. al. also investigated using electrochemical double-layer capacitance with an ion-gel material, achieving up to 2,400 nF cm^{-2} at room temperature, but with similarly high leakage currents.[13]

Despite these advancements, hafnia remains an excellent choice for catalytic condenser fabrication due to its high-temperature stability, large electrical breakdown window, high dielectric constant, and widespread availability.[14–16] This is reflected in extensive research aimed at improving the hafnia dielectric constant and reducing the leakage current in MOS devices and beyond. For instance, Gieraltowska et al. recently demonstrated that atomic layer deposition (ALD) parameters drastically impact hafnia layer quality, with increased growth temperatures boosting capacitance by up to 50%, while shorter ALD purge times reduce the measured dielectric constant.[17] Park et. al. successfully reduced the thickness of ALD hafnia films to 4 nm using a discrete precursor feeding method, maintaining electrical insulation but with a leakage current of ~1 mA at 1 V.[18] Kukli et. al. optimized deposition temperature to deposit 5 nm layers of hafnia with ~ 1 μA leakage at 1 V.[19] While these studies demonstrate the feasibility of fabricating ultrathin hafnia layers with insulating properties, leakage current remains a challenge for implementation in catalytic condensers for two main reasons: first, excess leakage resistively heats the device, complicating kinetic studies, and second, leakage current represents energy loss, reducing overall system efficiency.

In this work, we build upon foundational advances in catalytic condensers to enhance both their design and performance, focusing on two key areas: optimizing the hafnia dielectric layer to achieve ultrathin insulating layers (<10 nm) and redesigning the catalytic electrode geometry to maximize charge concentration within the catalytically active phase. By reducing the hafnia layer thickness, we increased the room-temperature capacitance of hafnia-based condensers by nearly an order of magnitude—from approximately 200 nF cm^{-2} to 2000 nF cm^{-2}. Simultaneously, we reduced the leak current at 1 V to below 100 nA for all fabricated thicknesses (sub-5 to 75 nm). To simplify the catalytic condenser architecture, we removed the carbon layer, providing a more straightforward model for future studies on charge dynamics and ensuring that the charge is localized within the catalytic layer. We further leveraged the electrical properties of SLG to concentrate charge within dispersed nanoislands of platinum, thereby increasing the charge per platinum atom. Given that in a parallel plate capacitor the charge is primarily localized at the interface between the conductor and the dielectric,[20] when a catalyst is deposited atop the conductor, the catalytic layer is positioned at least 3 Å (the thickness of SLG) away from the charged interface. This separation may be sufficiently large to reduce electronically-induced changes in catalytic activity. To address this potential limitation, we developed an alternative architecture—the blanket catalytic condenser—which inverts the traditional electrode geometry by directly depositing platinum nanoislands onto the hafnia layer and electrically connecting them with a top layer of SLG. To further enhance the catalytic layer design, we replaced the SLG with a 2–4 μm-thick porous carbon nanotube film, providing better access to the catalytic sites.

Results and Discussion

Carbon-free catalytic condensers with an ultrathin hafnia layer. The specific capacitance (nF cm^{-2}) of catalytic condensers follows the parallel plate capacitor equation, $C = k\varepsilon_0 A/d$ (Equation 1), where ε_0 and k are the permittivity of vacuum and the dielectric material, respectively, A is the area of the conductive plates, and d is the dielectric thickness. The modulation of electron density in the catalytic layer of catalytic condensers can be enhanced by increasing the capacitance. To achieve this, we fabricated hafnia (HfO_2) layers as thin as sub-5 nm, which drastically increased charge storage capacity. Figure 1a depicts this simplified catalytic condenser design where a slightly thicker film of only platinum (~3 nm) replaced the previously used carbon layer (~1 nm) with platinum on top (~1-2 nm). Scanning transmission electron microscopy (STEM) was used to investigate the morphology of the deposited films. As shown in Figure 1b, the STEM image shows that the hafnia layer is about 4.3 nm thick and uniform across the probed lamella domain (Figure S1). An amorphous interfacial layer (IL) exists between the hafnia and the positively-doped silicon (p-Si) layer, commonly formed during the ALD deposition process. This IL consists of hafnium silicates, with a gradient of composition from silicon-rich closer to the silicon substrate to hafnium-rich near the hafnia

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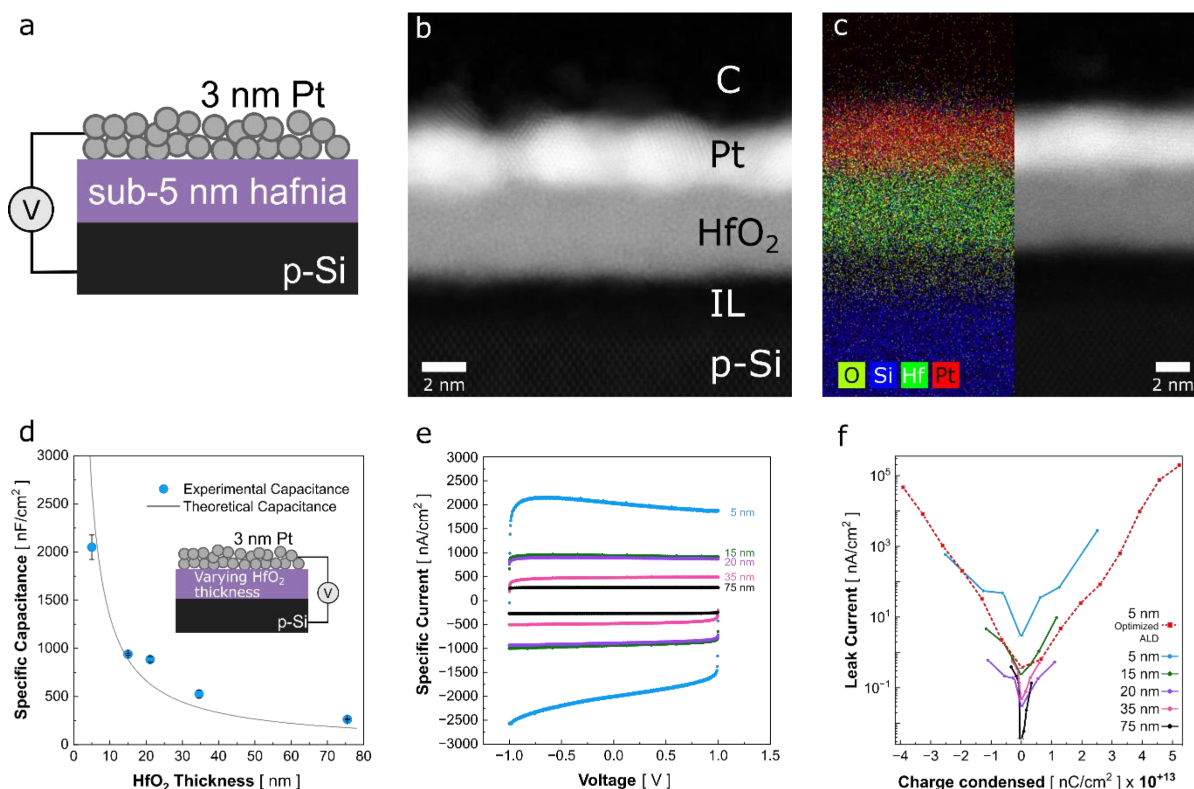

Figure 1. Fabrication and electrical characterization of ultrathin catalytic condensers. a) Illustration depicting the simplified condenser design without a carbon charge distributing layer. The condenser is composed of p-Si, variable thickness of HfO_2 as dielectric, and 3 nm of platinum (p-Si/HfO_2/Pt). b) STEM-HAADF image displaying the from top to bottom, carbon (C) protective layer, Pt, HfO_2, IL, and p-Si. c) STEM-EDS mapping (left) and corresponding STEM-HAADF (right) image showing the same element distribution as in b). The IL shows the co-presence of Hf and Si signals suggesting that its composition is a hafnium silicate, $Hf_xSi_{(1-x)}O_y$. d) Specific capacitance as a function of hafnia thickness ranging from 75 to 5 nm. The theoretical capacitance was calculated with parallel plate capacitor equation using a dielectric constant of 15. All the devices were fabricated with ALD at 275 °C and 1 second purges. e) Current-voltage (*I-V*) curves of representative devices in Figure 1d. Voltage windows [-1 V, + 1 V] and scan rate of 1 V s^{-1}. f) Leakage current as a function the charged condensed for all the thicknesses reported in Figure 1d. The red line shows the ALD optimized sub-5 nm device, with significantly lower leak current. Leak currents were truncated at 0 V since the value was not measured.

interface.[18,21–23] Additionally, the platinum layer exhibits a continuous polycrystalline phase, as indicated by the ordered arrangement of platinum atoms in Figure 1b. The high-angle annular dark field (HAADF) image in Figure 1b shows higher brightness for platinum in agreement with its higher atomic number, while a complementary bright-field (BF) image (Figure S2a-b) collected with a smaller scattering angle emphasizes phase contrast, with lighter elements appearing brighter. The BF image in Figure S2b helps better visualize the IL since oxygen possesses a lighter contrast with respect to silicon and hafnium.

Figure 1c shows the energy-dispersive X-ray spectroscopy (EDS) mapping analysis of the sample, confirming the elemental composition of the four layers. The topmost layer consists of carbon, used as a protective layer during the focused-ion beam process to prepare the TEM lamella. Below this layer are the platinum (red), hafnium (dark green), oxygen (light green), and silicon (blue) layers. The EDS mapping also confirms the hafnium silicate composition of the IL, as it is rich in oxygen and displays distinct signals for both hafnium and silicon.

As shown in Figure 1d, the thickness of the hafnia layer was systematically reduced from the conventional thickness of ~70 nm down to sub-5 nm. The 5 nm device exhibited a capacitance of approximately 2050 nF cm^{-2} when fabricated with a 1-second ALD purge time, representing an order of magnitude improvement compared to the 70 nm devices. We note that the

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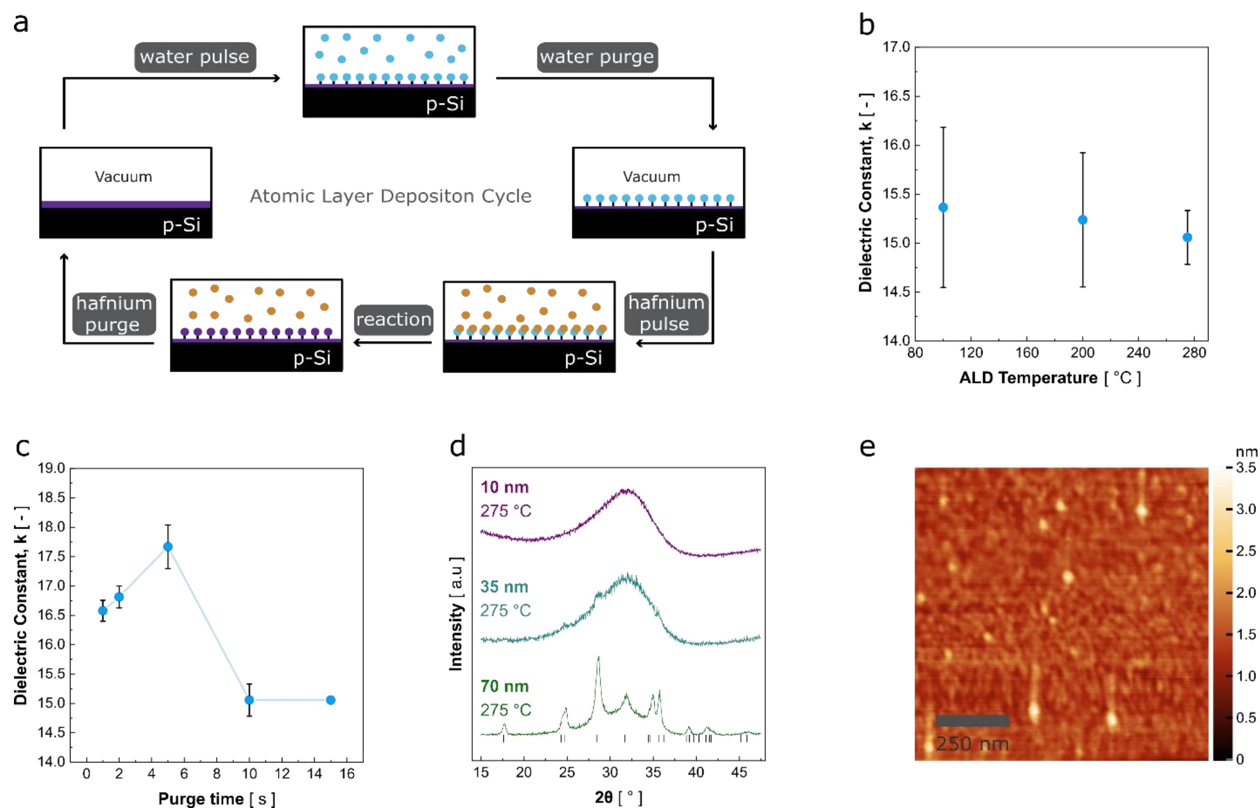

Figure 2. Optimization of atomic layer deposition process. a) Illustration of hafnia ALD steps. Throughout the process, there are alternating pulses of water (oxygen source) and tetrakis(dimethylamido) hafnium leading to layer-by-layer hafnia growth. b) Effect of deposition temperature on hafnia dielectric constant. Dielectric constant is calculated from capacitance and hafnia layer thickness using parallel plate capacitor geometry. All samples here have 10 s purge time. Standard deviation visualized as error bar. c) Effect of purge time on dielectric constant. Water purge and hafnium purge times were kept equivalent. Deposition is performed at 275 °C. Standard deviation visualized as error bars. d) Grazing Incidence XRD (Cu Kα, $\lambda = 1.5406$ Å) for as-synthesized hafnia films at 275 °C with thicknesses of 70, 35, and 10 nm. Pattern with vertical marks is for monoclinic hafnia phase. e) Atomic force microscopy (AFM) of hafnia film deposited at 275 °C with 10 second purges.

presence of the IL creates a capacitor with two dielectrics in series, which results in a total capacitance (C_{tot}) given by $\frac{1}{C_{tot}} = \frac{1}{C_{HfO_2}} + \frac{1}{C_{IL}}$ (Equation 2). Decoupling C_{HfO_2} and C_{IL} is challenging due to the difficulty of creating isolated, pure dielectric layers under the range of fabrication conditions explored. Renault et al. used a plasma-enhanced chemical vapor deposition method to deposit films of hafnium silicates, $Hf_xSi_{(1-x)}O_y$, with varying hafnium content, measuring dielectric constants in the range of 4 to 15 for different values of x.[24] Determining the exact capacitance of the IL is beyond the scope of this study; instead we measured an effective capacitance and dielectric constant resulting from the composite hafnia-IL layers. We note that as the hafnia thickness increases, the IL has less influence on the total capacitance. Note S1 provides detailed calculations showing that the IL cannot be solely composed of silica (SiO_2), as the maximum capacitance of a device with 2 nm of SiO_2 in series would be lower than what we measured for the p-Si/sub-5 nm HfO_2/Pt stack. We thus conclude that the IL is likely a composite of hafnium silicate with a dielectric constant higher than that of SiO_2.

The electronic properties of the condensers with various thicknesses were assessed through current-voltage (*I-V*) curves, as shown in Figure 1e. Cyclic voltammetry (CV) measurements were performed with a voltage range of +1 V to -1 V at a scan rate of 1 V s^{-1}, with all condensers exhibiting predominantly capacitive behavior. The corresponding leakage current as a function of the condensed charge per area is shown in Figure 1f. Devices with hafnia layer thicknesses greater than 5 nm exhibited extremely low leakage currents, consistently less than 10 nA cm^{-2}. The 5 nm-thick devices exhibited a low leakage current of < 70 nA in the

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same charge condensation window. However, the leakage current increased to 3000 nA at +2 V and 600 nA at -2 V, corresponding to a condensed charge of 2.5 x 10^{+13} e^-/h^+ cm^{-2}. Although the leakage currents at ±2 V are relatively high, these values are insufficient to induce any significant amount of resistive Joule heating.[13] Nonetheless, the leakage current still represents a continuous energy loss, as a constant supply of current is required to maintain the voltage difference. Therefore, minimizing leakage current or operating under conditions that balance sufficient charge condensation with low leakage is crucial to optimize energy efficiency. After optimizing the ALD process (*vide infra*), the sub-5 nm devices were refabricated under optimal conditions, resulting in consistent, low leak performance (red line in Figure 1f) with a similar capacitance of 2040 nF cm^{-2}. The sub-5 nm hafnia film achieves an equivalent oxide thickness (EOT) of 1.1 nm, meaning it provides the same capacitance as a 1.1 nm-thick silica layer. EOT is a standard metric used to compare the effective thickness of dielectric layers based on their capacitance. By comparing the performance of these hafnia layers with state-of-the-art hafnia films in MOS capacitors, we find that our films exhibit some of the lowest leakage currents at 1 V for an EOT of 1.1 nm (Figure S3). [25]

Using the 3 nm platinum layer as both an electrode and a catalyst simplifies the condenser design by eliminating the need for a carbon layer to distribute charge, while also ensuring that the bottom surface of the active (platinum) layer is charged.

Optimization of atomic layer deposition process. Optimization of the ALD process is critical to improving the performance of hafnia-based catalytic condensers. Figure 2a illustrates the five key steps of each ALD cycle. The process begins with the adsorption of a water monolayer on the p-Si surface, where a more uniform and complete monolayer results in higher-quality oxide films. After purging the water under vacuum, the hafnium precursor (tetrakis(dimethylamido) hafnium, TDMAH) is introduced, reacting with the adsorbed water to form HfO_2. Deposition temperature influences both adsorption and reaction kinetics. To explore this effect, we fabricated a series of 15-nm-thick hafnia catalytic condensers, keeping the purge time constant at 10 seconds but varying the ALD chamber temperatures. The specific capacitances of the resulting films were used to calculate the dielectric constant. As shown in Figure 2b, no significant difference in dielectric constant was observed between condensers fabricated at 100 °C and those at 275 °C. This result is in contrast with the findings by Gieraltowska et al., where higher deposition temperatures lead to significantly higher hafnia dielectric constant values.[17] This suggests that the behavior of hafnia at ultrathin interfaces may differ from its bulk properties, or that the lower dielectric constant value of the IL hinders the extraction of the pure k_{hafnia}. We also note that our measured dielectric constant is the bulk value of both hafnia and the IL. For subsequent experiments, we selected the deposition temperature of 275 °C, as it yielded a smaller standard deviation in dielectric constant, providing more consistent results across samples.

In ALD, achieving the optimal chamber purge time is essential for high-quality film formation. If the purge time is too short, precursor oxidation reactions may occur in the vapor phase or lead to multilayers on the surface, while long purge times can deplete the surface monolayer, resulting in incomplete coverage. For a series of catalytic condensers fabricated at 275 °C, Figure 2c shows the hafnia dielectric constant for purge times ranging from 1 s to 15 s. In our devices, the ALD growth rate depended on purge time (Figure S4), with longer purge times resulting in lower growth rates. Further, the dielectric constant and resulting leak current were strongly influenced by film thickness (Figure S5). Accordingly, to ensure consistent film thicknesses across devices, the number of ALD cycles was adjusted so that all films were within 1 nm of each other. At 275 °C, a 5-second purge time generated the highest dielectric constant, nearly 20% higher than those obtained at longer purge times. This result reflects the tradeoff between short and long purge times for monolayer coating quality. Indeed, when using a 15-second purge time, only one out of four devices worked successfully as a capacitor (explaining the absence of the error bar), likely due to partial monolayer depletion, which resulted in a defective hafnia film. We note that the optimal 5-second purge time also resulted in significantly lower leak currents. As shown in Figure 1f, when comparing the thinnest device fabricated with a 1-second purge time (blue) to that with a 5-second purge time (red), the latter exhibited approximately an order of magnitude lower leak current at 1 V. This improvement enables the condensation of 4.6 x 10^{13} charges cm^{-2} while maintaining a leakage current below 100 μA cm^{-2} where resistive Joule heating is negligible.[13]

To further investigate the differences between hafnia layers deposited under different ALD conditions, grazing incidence X-ray diffraction (GIXRD) was performed on hafnia films deposited at different temperatures, purge times, and film thicknesses (Figures 2d and S6). Films with a 75 nm thickness exhibited a crystalline monoclinic hafnia phase. However, reducing the thickness to 35 nm led to a significant decrease in crystallinity (Figure 2d). Films thinner than 35 nm were either amorphous or had crystallite sizes too small to be

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detected by GIXRD (Figure 2d top spectrum). STEM-HAADF in Figure S7a-b shows that the hafnia film is composed of crystalline and amorphous domains. Namely, on the left side of the image, an atomic short-order range is detectable while on the right side, no clear crystalline domains were observed. This was a general trend across all the hafnia layer that was probed, alternating crystalline and amorphous domains. To confirm that the crystallinity of such thin films could be quantified using GIXRD, a 12 nm hafnia layer was calcined at 450 °C, resulting in the formation of a crystalline monoclinic phase (Figure S6b). GIXRD was also used to investigate the effects of temperature (100 °C and 275 °C) and ALD purge time (1, 2, and 10 s) on hafnia crystallinity (Figures S6a and S6c). In all cases, the films displayed XRD patterns consistent with amorphous structures or small, undetectable crystallite sizes.

Surface morphology and roughness are important parameters when depositing nm-thick continuous films. To assess the impact of deposition parameters on surface morphology, atomic force microscopy (AFM) was performed on samples deposited at 100 °C, 200 °C, and 275 °C. Figure 2e shows the exceptionally smooth AFM trace over a 1 μm^2 area for a hafnia film deposited at 275 °C with 10-second purges. For all temperatures, the films exhibited a consistent trend, with a mean roughness of approximately 0.1 nm (Figure S8 and Note S2). These measurements suggest that the absence of peaks in the GIXRD results could be attributed to the small crystallite size. Short-range order, however, can still be detected using techniques like STEM (Figure S7).

After optimizing the ultrathin hafnia layers, the next goal was to maximize the charge per platinum atom. Using the simplified catalytic condenser fabrication procedure (p-Si/HfO_2/Pt) illustrated in Figure 1, we found that a platinum layer thickness of 3 nm is the minimum electrode thickness required to maintain a continuous conductive layer. Reducing the platinum thickness below this threshold results in a marked decrease in capacitance because of insufficient conductivity in the platinum layer.

Single-layer graphene devices. SLG is an excellent candidate for reducing the overall amount of catalytic material while enhancing the charge perturbation per atom. By depositing a high-quality, electrically conductive SLG sheet on top of the hafnia layer, it becomes possible to disperse isolated catalyst nanoislands across the graphene surface, significantly improving their dispersion (Figure S9). The transfer of SLG from the copper support to the desired substrate is a tedious process prone to induce cracks and tears that alter the geometry and electrical properties of graphene.[26–28] Additionally, the state-of-the-art polymethylmethacrylate (PMMA) graphene transfer process often leaves behind surface residues, even after extensive cleaning treatments.[29–31] We adapted a paraffin-based transfer method, which was shown to improve cleanliness and reduce electrical resistance compared to traditional PMMA processes.[32]

As illustrated in Figure 3a, commercial SLG on copper was coated with a thin layer of a solution of paraffin and cyclohexane. Copper etching with a solution of iron chloride ($FeCl_3$) followed by acid and water washing steps was carried out before transferring the SLG/paraffin onto the p-Si/HfO_2.[33] After drying (Figure 3b) the paraffin was removed by soaking the entire device in hexane overnight, which yielded an indistinguishable layer except for the blade-cut edges (Figure 3c). The use of a solution instead of solid paraffin greatly simplifies the coating step as no substrate heating is required.

The quality of the graphene transfer process was evaluated using Raman spectroscopy to monitor for defects introduced after the transfer onto the p-Si/HfO_2 substrate. As shown in Figure S10, the graphene on copper was mostly composed of single layers, indicated by an I_{2D}/I_G ratio >2 (Table S1). Additionally, the graphene was defect-free, as no D peak was observed in any of the measurements. After transfer, the graphene maintained its defect-free nature and single-layer morphology, as confirmed by similar Raman results (Table S1).

Figure 3d shows the capacitance of p-Si/HfO_2/SLG devices with hafnia thicknesses ranging from 5 to 70 nm (cyan color). At hafnia thicknesses greater than 20 nm, measured capacitances matched the theoretical capacitances expected for this geometry with a dielectric constant of 15. However, at ultrathin hafnia thicknesses, the specific capacitance of SLG-only devices was lower than the theoretical geometrical capacitance (gray line), Equation 1, with deviations up to 50%. Despite this discrepancy, capacitance was still more than an order of magnitude higher than previously reported values for similar devices.[7] The discrepancy between theoretical capacitance and the capacitance of SLG-based devices increased as the thickness of the hafnia layer decreased.

We hypothesized that the observed discrepancy could be attributed to the quantum capacitance of graphene, which is constrained by its limited density of states.[34,35] When the overall capacitance of a system is influenced by the density of states of one electrode, the

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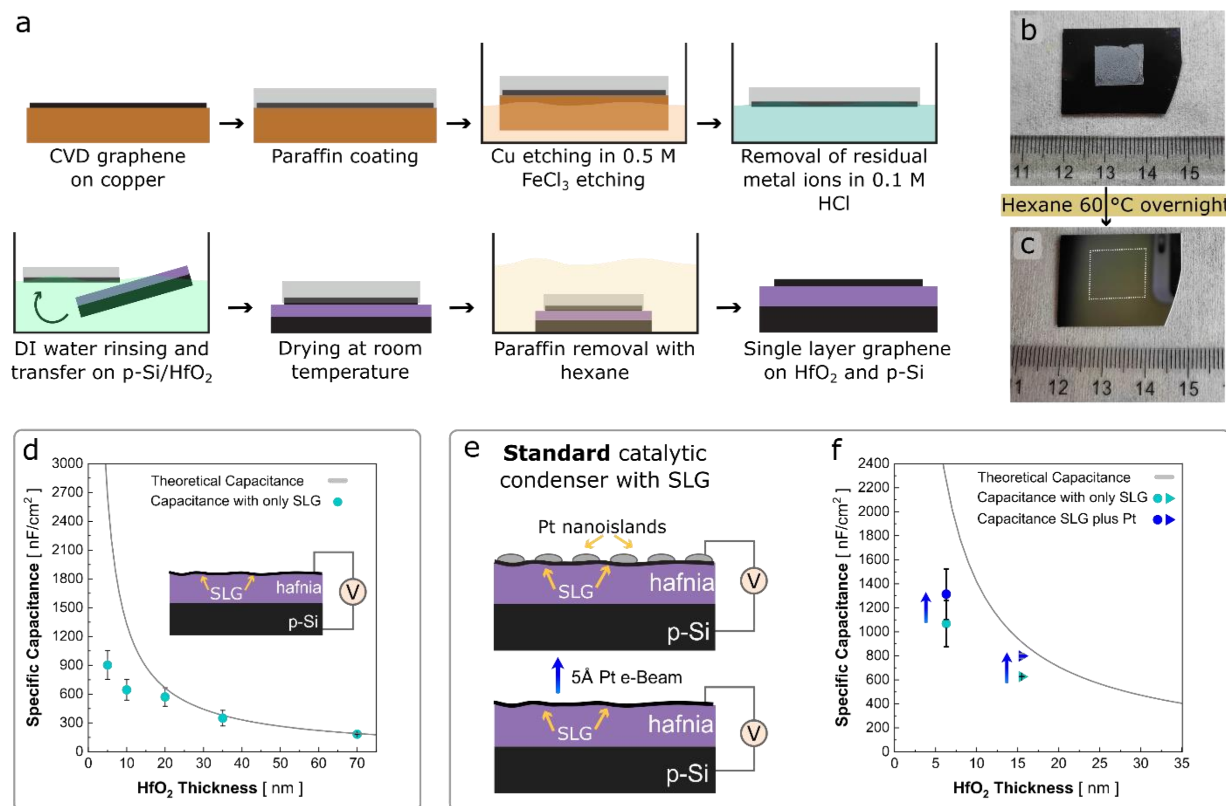

Figure 3. Blanket and standard catalytic condenser fabrication with SLG and CNT films. a) Illustration of SLG transfer process. b) Image of SLG coated with paraffin on p-Si/HfO_2. c) Same device as in b) after removal of paraffin with a hexane bath at 60 °C overnight, the dotted-squared white line indicate the faded edges of the SLG contour. d) Specific capacitance of p-Si/HfO_2/SLG catalytic condensers with varying HfO_2 layer thicknesses. The gray line indicates geometrical capacitance with k = 15. e) Illustration of fabrication of standard condenser architecture (p-Si/HfO_2/SLG bottom cartoon and p-Si/HfO_2/SLG/Pt top cartoon). f) Specific capacitance of standard catalytic condensers before (teal) and after (dark blue) the deposition of 0.5 nm of platinum.

total measured capacitance can be described by $\frac{1}{C_{measured}} = \frac{1}{C_{geom.}} + \frac{1}{C_q}$ (Equation 3), where $C_{geom.}$ is calculated from the parallel plate capacitor geometry and dielectric constant, and C_q is the potential-dependent quantum capacitance of graphene- which accounts for the changing chemical potential of an electron in graphene.

The data in Figure 3d support this hypothesis. For thicknesses larger than 20 nm, the capacitance of SLG devices aligns well with the geometrical capacitance, indicating $C_q >> C_{geom.}$ However, as $C_{geom.}$ increases with decreasing hafnia thickness, the capacitance of the graphene-based devices shows a linear trend with thickness, *d*, rather than the expected d^{-1} relationship, indicating $C_q \sim C_{geom.}$ When 0.5 nm of platinum was deposited on top of the p-Si/HfO_2/SLG (Figure 3e), only a partial recovery (~25% increase) of the theoretical geometrical capacitance was observed, suggesting that a fraction of the condensed charge resides in the disconnected platinum nanoislands (Figure 3f), while the majority of the charge remains concentrated in the SLG layer, which is closest to the dielectric. The partial recovery of capacitance after platinum deposition can be partly attributed to the limited coverage of the surface, with the platinum forming nanoislands that cover only about 65% of the area. (Figure S9).

Blanket catalytic condensers. In a parallel plate capacitor, the condensed charge is located at the interface between the electrode and the dielectric due to electrostatic attractive forces between the charges in the two plates.[20] In the catalytic condenser design described above, the charge stored in the platinum layer is significantly less than the total charge stabilized by the hafnia, as most of the charge is localized in the bottom graphene layer. Similarly, even when using the

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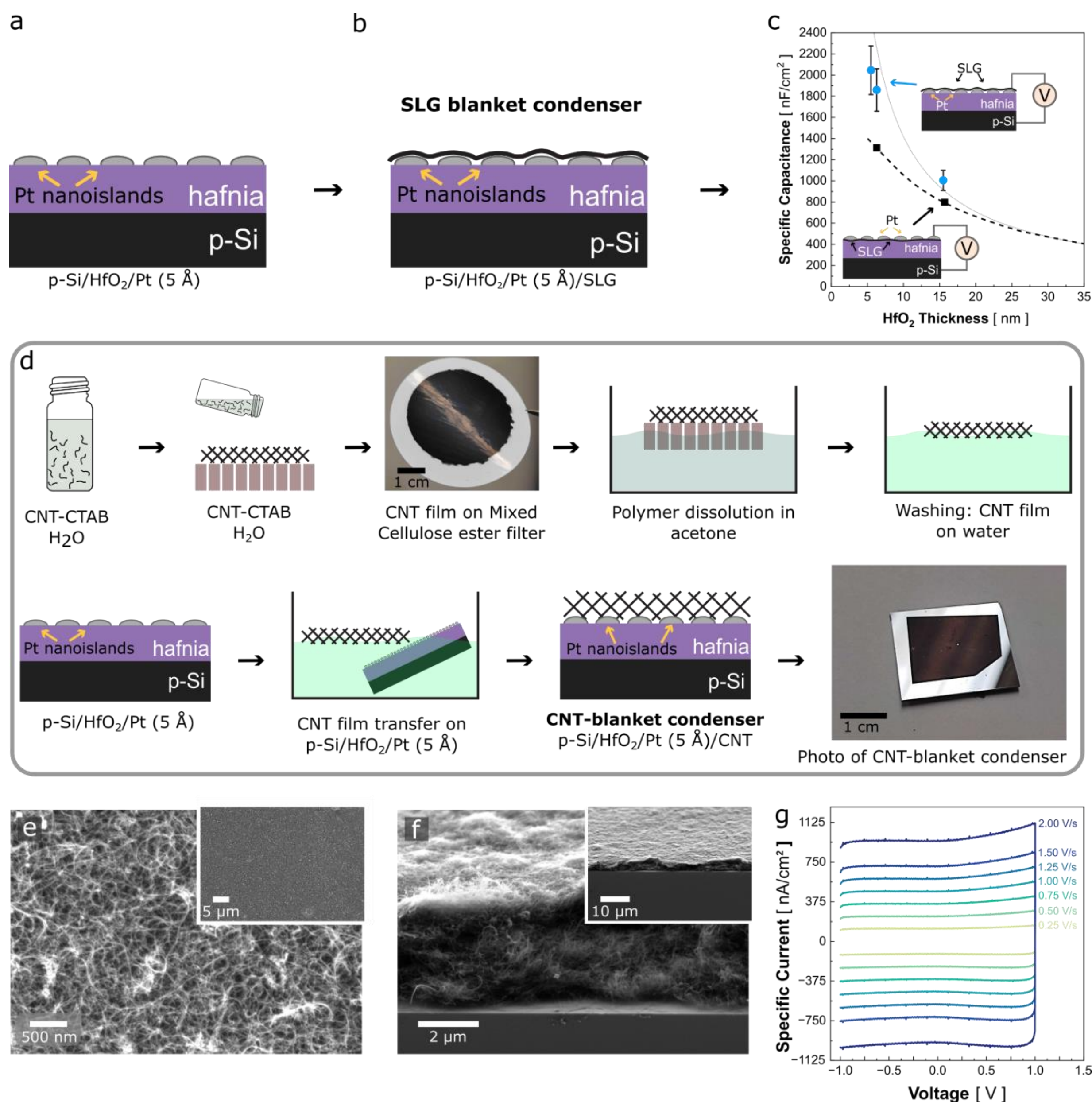

Figure 4. Blanket catalytic condensers. a) Ensemble of p-Si/HfO_2/Pt, the platinum layer does not form an electrically conductive layer. b) Blanket catalytic condenser with SLG as an electrically connecting layer for dispersed platinum nanoislands. c) Specific capacitance of blanket condensers (p-Si/HfO_2/Pt/SLG, top-right cartoon) with varying thicknesses of HfO_2 (cyan data points). Gray line represents theoretical capacitance for k = 15. Black data is for standard condenser architecture with SLG (p-Si/HfO_2/SLG/Pt, bottom-left cartoon), the dashed line it is for visual aid. d) Illustration of porous CNT blanket condenser fabrication process. e) Low (inset) and high mag top-view SEM images of CNTs on top of p-Si/HfO_2/Pt. e) Low (inset) and high mag cross-sectional SEM images of CNTs on top of p-Si/HfO_2/Pt. The images were taken with a tilt of 45°, but the scale bar was adapted, dividing it by cos(45°). f) Cyclic voltammetry curves under various scan rates for the CNT-based blanket condenser fabricated on a 30 nm-thick hafnia layer.

simplified geometry shown in Figure 1, according to the Thomas-Fermi screening theory, the charge is confined to interatomic distances, limiting the penetration of charge into the outer, catalytically active surface.[36]

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To address this limitation, we developed "blanket catalytic condensers", an alternative architecture where the active catalytic phase (e.g., platinum) is now in direct contact with the dielectric (Figure 4a) and the SLG covers the active phase, ensuring electrical conductivity between the disconnected platinum nanoislands (Figure 4b). Capacitance measurements of blanket catalytic condensers at hafnia thicknesses of 6 and 15 nm (Figure 4c, cyan data) show that these devices achieve higher capacitances than standard condensers with platinum on top of graphene, aligning closely with the expected geometrical capacitance values. This demonstrates that blanket catalytic condensers allow the dispersed platinum nanoislands to achieve the maximum condensable charge for a given hafnia thickness. Moreover, this result also indicates that the graphene transfer process is robust and yields a graphene area in alignment with the geometrical one, meaning the entire area is electrically connected.

However, because SLG is impermeable to even the smallest gas molecules (e.g., helium, with a kinetic diameter of 0.26 nm), [37] SLG-based blanket condensers are suitable primarily for spectroscopic measurements rather than catalytic applications. To adapt the blanket catalytic condenser for catalysis applications, we replaced the non-porous SLG layer with a carbon nanotubes (CNTs) film. The CNT film fabrication process is illustrated in Figure 4d. CNTs were dispersed in water *via* sonication with cetyltrimethylammonium bromide (CTAB) as a surfactant. The dispersion was vacuum filtered onto a mixed cellulose ester membrane (MCE) yielding a homogenous coating onto the filter. After the MCE membrane was dissolved in acetone, the CNT film was transferred to a water bath for washing. Finally, The CNT film was scooped with a p/Si/hafnia/Pt (5 Å) ensemble. The final device displayed a uniform CNT film (Figure 4d).

Figure 4e presents scanning electron microscopy (SEM) micrographs of the CNT film, displayed at both high and low magnifications (inset). The images reveal a uniform coating with a porous structure, where individual carbon nanotubes can be distinctly identified. The entanglement of the CNTs contributes to the film's mechanical stability, demonstrating strong adhesion properties as the film remained intact even after immersion in water. This robustness suggests potential applicability in liquid-phase reactions. The thickness of the CNT film can be adjusted by varying the concentration of CNTs in the solution. We fabricated films ranging from 2 to 4 μm in thickness, which were uniform across the entire sample (Figure 4f).

The electrical properties of the CNT-based blanket catalytic condenser were evaluated using CVs following the same protocol as for previous condenser architectures. The device exhibited a capacitance of approximately 500 nF cm^{-2} with a 30 nm hafnia film (Figure 4g), which is in good agreement with the capacitance values observed in earlier catalytic condenser designs (Figure 1d).

Conclusions. Catalytic condensers with an ultrathin (sub-5 nm) hafnia layer were successfully fabricated, increasing the capacitance from the conventional ~200 to ~2000 nF cm^{-2}, enabling the condensation of up to 4.6 x 10^{+13} charges cm^{-2} without significant current leakage. By using a 3 nm platinum layer as both the electrode and catalyst, we eliminated the need for a carbon layer, thus simplifying the fabrication process. While this catalytic condenser geometry provides a more straightforward model for studying charge dynamics, we also developed additional architectures designed to maximize the ratio of condensed charge to platinum atoms.

A simplified graphene transfer process using paraffin as the mechanically reinforcing layer was developed, allowing SLG to serve as the charge distributor. This advancement enabled the deposition of a very thin (5 Å) layer of platinum that would otherwise lack sufficient electrical conductivity. Quantum capacitance effects were observed in graphene-only devices (p-Si/HfO_2/SLG) with ultrathin hafnia, resulting in capacitances lower than those precited by parallel plate models or observed with platinum-only electrodes.

To ensure that the condensed charge is concentrated in the catalytic active phase, we introduced the concept of blanket catalytic condensers. In this architecture, a minimal amount of the catalyst (0.5 nm) was directly deposited onto the dielectric, with its electrical connection maintained by transferring an SLG film on top. This approach yielded the expected geometrical capacitance. Finally, we adapted the blanket condenser concept for application in catalysis by replacing the SLG with an ex-situ fabricated film of porous CNTs. We anticipate that the high capacitance and low leak currents achieved through the optimization of ultrathin hafnia, combined with the blanket catalytic condensers architecture, will significantly enhance charge modulation at catalytic sites.

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Methods:

ALD: All catalytic condensers were fabricated on 4" p-doped silicon wafers (p-Si) (WaferPro, resistivity ≤ 0.005 Ohm-cm). HfO_2 was deposited on the p-Si with a Cambridge Nanotech Savannah 200 ALD machine. The ALD process involved alternating pulses of water (t = 15 ms) and tetrakis(dimethylamido) hafnium (TDMAH, t = 120 ms) with purge times between pulses varying from 1 to 15 s and at temperatures ranging from 100 to 275 °C. To achieve various hafnia thicknesses, the number of ALD cycles was varied from 50 to 750, with an average deposition rate observed of 0.9 Å per cycle.

Ellipsometry: Hafnia thicknesses were measured using a Semilab SE2000 ellipsometer. Measurements were collected at incidence angles from 65-75 degrees. Semilab's spectroscopic ellipsometry analyzer (SEA) software was used to model the stack as a single HfO_2 layer. Thickness measurements across all four wafer quadrants had measured thicknesses within 0.1 nm.

E-Beam: Platinum was deposited at 0.2 Å s^{-1} with an electron beam evaporator system (AJA International ATC-E HV Series). The wafer was divided into multiple ~ 2 cm^2 condensers with the use of a polyimide shadow mask (Figure S11).

Graphene transfer: Monolayer graphene grown by CVD on copper foil (General Graphene Corporation) was cut into ~ 2 cm^2 pieces and spin-coated with a mixture of 75% cyclohexane and 25% paraffin heated to 50 °C. Subsequently, the copper foil was etched using a bath of 0.5 M $FeCl_3$ for 1 hour. The remaining metal ions were removed using a solution of 0.1 M HCl for 1 hour. Finally, the graphene was transferred to a DI water bath and scooped onto p-Si/HfO_2. After drying overnight, the paraffin top layer was removed using hexane heated to 60 °C. Details for the main steps are highlighted in Figure S12.

CNT film fabrication and transfer: Multiwalled carbon nanotubes (Cheaptubes), with outer diameters of less than 8 nm and lengths ranging from 10 to 30 µm, were dispersed in water containing CTAB (0.01% w/w) relative to the CNT mass. The dispersion was achieved via sonication to create a 10% solution. Small aliquots (200 µL) were taken from this mother solution and further diluted in water (200 mL) and further sonicated for 30-60 min. The solution was finally filtered onto a Mixed Cellulose Ester filter (MCE) with 200 nm pores (Merck). Upon drying the filter was dissolved in acetone and the CNT film was transferred onto the p-Si/HfO_2/Pt.

Capacitance quantification: Capacitance measurements were performed at room temperature on a custom stage (Figure S13) where aluminum foil contacts the bottom electrode, and a conductive rubber is used to make gentle contact with the top electrode. Capacitance was measured with cyclic voltammetry from -1 to +1 V (scan rate 1 V s^{-1}, Gamry Interface 1010B Potentiostat). Gamry's surface measurement mode, designed for measuring capacitance, was used to integrate the total amount of charge passed during each voltage step.

Raman: Raman measurements were carried out using a Renishaw Invia Reflex Raman Confocal Microscope equipped with a 532 nm wavelength laser operating at 50 mW power. A manual background subtraction was performed using a spline function before analyzing the D, G, and 2D peaks of graphene.

XRD: Grazing incidence X-ray diffraction (GIXRD) measurements were performed using a Rigaku Smartlab diffractometer equipped with a scintillation counter 0D detector and a copper target operating at 45 kV and 200 mA, utilizing Cu Kα radiation (λ = 1.5406 Å). The measurements were conducted in parallel beam mode, with an incident angle of 0.5° and an incident slit height of 0.06 mm.

AFM: AFM profiles were measured by an Asylum Research Cypher VRS atomic force microscope using the force-modulation technique (tapping mode). Probes were standard Si cantilevers purchased from Oxford instruments with a spring constant of 26 N m^{-1}. The measurements of the mean surface roughness were acquired from a few randomly chosen sections in the AFM images of 1 µ x 1 µ area.

SEM: SEM images were taken on a high-resolution Zeiss Merlin at 1-2 kV and 149 pA current. Everhart Thornley Secondary Electron Detector was employed and the working distance ranged from 2 to 7 mm.

FIB lamella preparation: The focused-ion beam (FIB) lamella was prepared using a FEI Helios Nanolab 600 Dual Beam System. To protect the p-Si/HfO_2/Pt sample, a carbon protective layer was first deposited using the electron beam, forming a box with dimensions of (2, 15, 2) µm (x, y, z). This was followed by an additional carbon layer of the same size, deposited using the ion beam for enhanced protection. Rough trenching around the area of interest was performed using gallium ions at 30 kV and 21 nA, while the final thinning cuts were made at 5 kV and 47 pA to achieve the desired lamella thickness.

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STEM-HAADF: High-angle annular dark field (HAADF) STEM imaging, along with energy dispersive spectroscopy (EDS), were performed using an aberration-corrected Thermo Fisher Scientific Themis G3, equipped with Super-X EDS detectors. The imaging and spectroscopy were carried out at 200 kV, with a probe convergence semiangle of 19 mrad and beam current ranging from 80 to 150 pA. The HAADF imaging utilized an annular collection angle of 70-200 mrad.

Conflicts of interest: There authors declare no conflicts of interest.

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