Interface-Engineered Atomic Layer Deposition of 3D $Li_4Ti_5O_{12}$ for High-Capacity Lithium-Ion 3D Thin-Film Batteries

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Keywords: 3D Li-ion microbatteries, atomic layer deposition, high capacity electrodes, high power, lithium titanium oxide (LTO)

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Abstract:

Upcoming energy-autonomous mm-scale Internet-of-things devices require high-energy and high-power microbatteries. On-chip 3D thin-film batteries (TFBs) are the most promising option but lack high-rate anode materials. Here, $Li_4Ti_5O_{12}$ thin films fabricated by atomic layer deposition (ALD) are electrochemically evaluated on 3D substrates for the first time. The 3D $Li_4Ti_5O_{12}$ reveals an excellent footprint capacity of 20.23 µAh cm^{-2} at 1 C. The outstanding high-rate capability is demonstrated with 7.75 µAh cm^{-2} at 5 mA cm^{-2} (250 C) while preserving a remarkable capacity retention of 97.4 % after 500 cycles. Planar films with various thicknesses exhibit electrochemical nanoscale effects and are tuned to maximize performance. The developed ALD process enables conformal high-quality spinel (111)-textured $Li_4Ti_5O_{12}$ films on Si substrates with an area enhancement of 9. Interface engineering by employing ultrathin AlO_x on the current collector facilitates a required crystallization time reduction which ensures high film and interface quality and prospective on-chip integration. This work demonstrates that 3D $Li_4Ti_5O_{12}$ by ALD can be an attractive solution for the microelectronics-compatible fabrication of scalable high-energy and high-power Li-ion 3D TFBs.

1. Introduction

Self-powered mm-scale Internet-of-Thing (IoT) devices could enable decentralized wireless sensor networks, reducing the energy consumption, maintenance, and costs of environmental monitoring and industrial automation. Autonomous IoT systems are forecasted to reach a global market of USD 85 billion in 2024.[1] The ongoing miniaturization of electronic devices requires on-chip energy storage solutions with similar geometrical dimensions.[2] The main challenge of microsized batteries is to maintain both high-energy and high-power capability. Liquid-based Li-ion batteries have a limited scaling ability due to the hermetic packaging requirements preventing leakage of the flammable and moisture-sensitive electrolyte.

TFBs containing solid-state electrolytes and binder-free electrodes offer tremendous potential to fulfill the mm-scale device dimensions. Manufacturing of TFBs can be conducted with Si technology, enabling on-chip integration to replace standard supercapacitors with high-leakage currents.[3] TFBs exhibit high-power density, long cycle life, high-temperature and chemical stability, and low self-discharge.[4] However, the low film thickness enabling the short Li diffusion length also results in more pronounced interfacial challenges and an overall low energy density.[4] The most promising option to improve the energy density per footprint

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area is the so-called 3D TFB. The solid-state battery layer stack is coated over a surface area-enhanced microstructured substrate.[5,6] After the conceptional introduction of 3D TFBs in 2004, the first functional full cell was demonstrated by Pearse et al. in 2018.[6,7] The current state, remaining challenges, and prospective developments of 3D TFBs were summarized by Moitzheim et al.[8]

ALD is the most suitable technology for the required conformal and pinhole-free deposition on highly structured substrates.[9,10] Furthermore, the sequential and self-limiting surface reactions of this vapor-phase technique enable the stoichiometric control of nanometer-thin films. Although ALD is an established and well-understood technology in the integrated circuit industry, manufacturing Li compound thin films remains challenging.[11,12,13] A wide variety of Li-containing cathode and solid-state electrolyte materials were manufactured by ALD and electrochemically studied.[8,12–14] $LiMn_2O_4$, $LiFePO_4$ and LiPO(N) were examined in 3D TFB half cells.[7,15–17] However, the stage of development of Li-containing ALD anodes is behind. The first electrochemical investigation of planar LTO films by ALD was demonstrated recently by Speulmanns et al.[18] Only one electrochemical examination of LTO films on a microstructured substrate was reported.[19] However, the typical poor conformality of the applied metal-organic chemical vapor deposition (MOCVD) resulted in a low footprint capacity increase. The most advanced anode material for 3D TFBs is the closely related TiO_2.[16,20–22] High capacities of 370 µAh cm^{-2} for thick 155 nm TiO_2 with a high area-enhancement factor (AEF) of 53 were demonstrated but suffered from poor C-rate performance.[16] The best rate capability was accomplished by Cl-doped amorphous TiO_2 films.[21] The 100 nm films deposited on structures with an AEF of 21 reached 80 % of the maximum capacity of 249 µAh cm^{-2} at 2 C and 37 % at 20 C. A satisfactory high-power anode for 3D TFBs still needs to be developed.

Spinel lithium titanate ($Li_4Ti_5O_{12}$, LTO) is a promising anode material for 3D TFBs due to its high-power capability, safety, cycle stability, and “zero-strain” behavior.[23] 3D Li ion diffusion pathways within the material are another advantage.[24] The high degree of freedom for diffusion is particularly beneficial on microstructured substrates with various surface orientations. Upon lithiation, the material undergoes a phase transition to the rocksalt-like $Li_7Ti_5O_{12}$ with a minimal volume change below 0.2 %.[25] Thereby, film cracks, delamination, and interfacial stress in the 3D structures can be impeded and a high Li-ion insertion/extraction reversibility is enabled.[26] The intercalation of Li ions at a flat voltage of

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around 1.55 V versus Li^+/Li leads to high safety by eliminating the risk for Li dendrite formation and organic electrolyte reduction.[27] Three Li ions per formula unit can be intercalated in the typical potential range of 1 to 2.5 V versus Li^+/Li, leading to a moderate theoretical capacity of 175 mAh g^{-1} or around 600 mAh cm^{-3}. Drawbacks are the low electronic and ionic conductivities of the endmembers of LTO.[23,28] The slow intrinsic kinetics can be improved by nanoscaling, doping, and surface coating.[23] However, the demonstrated excellent high-power performance of LTO can be attributed to the facile Li-ion transport mediated by metastable intermediates along the two-phase boundaries with low transport energy barriers.[29]

The first successful fabrication of $Li_xTi_yO_z$ films by ALD was reported several years ago.[30,31] Lithium-*tert*-butoxide (LTB) and lithium hexamethyldisilazide (LiHMDS) are the most common precursors for ALD of Li-containing thin films. Spinel LTO films were achieved by classic supercycle ALD depending on the precursor combination and ratio.[31] A general challenge of fabricating Li-containing films is chemical vapor deposition (CVD)-like growth due to the so-called "water reservoir effect".[32] Bönhardt et al. introduced a three-step ALD process with LTB to mitigate this effect and achieved excellent conformality in high-aspect-ratio (HAR) structures.[33] The first electrochemical investigation of LTO films was performed in our previous study employing a 3-step ALD process with LiHMDS.[18] The planar films showed excellent electrochemical properties, but several issues occurred.[18,34] The incorporation of Si from the LiHMDS precursor into the film for long pulse times resulted in a CVD-like growth regime and subsequent poor conformality in HAR structures.[18] For LiPON fabrication, LiHMDS revealed inferior conformality compared to LTB.[35] Furthermore, the complete crystallization of ALD LTO required significantly longer annealing times on TiN current collectors than on SiO_2 substrates. The necessary long high-temperature exposure during the annealing process could lead to film delamination, film impurities, and inferior electrochemical properties.[18,34]

In this work, we systematically examine the electrochemical performance of interface-engineered ALD LTO thin films on area-enhanced Si wafers for the first time. A three-step ALD process with LTB with a saturated growth per cycle (GPC) is successfully developed and optimized towards high conformality in microstructures, enabling 3D TFBs. The impeding influence of the TiN current collector on the crystallization behavior of ALD LTO is suppressed by introducing an AlO_x interlayer. High-quality spinel (111)-textured LTO films

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with different thicknesses from 25 to 75 nm are manufactured to evaluate electrochemical nanoscale effects. The 50 nm LTO exhibits the best compromise of footprint capacity and current with outstanding high-rate cyclability. 3D LTO with an AEF of 9 demonstrates the combination of high footprint capacity and high-power capability while maintaining the excellent cycle life.

2. Results and Discussion

The key aspect of this study comprises the fabrication and assessment of 3D LTO anodes with larger footprint capacities than planar films while retaining high power capabilities. The Si-technology-compatible manufacturing of 3D TFBs is enabled by utilizing ALD and microstructured Si substrates. **Figure 1** illustrates the proposed strategy to reach the goal of the first 3D LTO electrode by ALD. In the first step, the 3-step ALD process is developed and optimized towards a high GPC. The second part of this study consists of the investigation of nanoscale effects on the electrochemical performance of planar LTO. An optimum film thickness must be identified since enhancing the footprint capacity by thicker layers limits the power capability. The role of surface roughening on intensified adverse storage mechanisms is determined. Interface engineering by an interlayer is introduced to reduce the required LTO crystallization time and improve the electrochemical properties. As a third step, 3D LTO with high energy and power densities is fabricated employing a further optimized ALD process on 3D Si substrates with high AEFs.

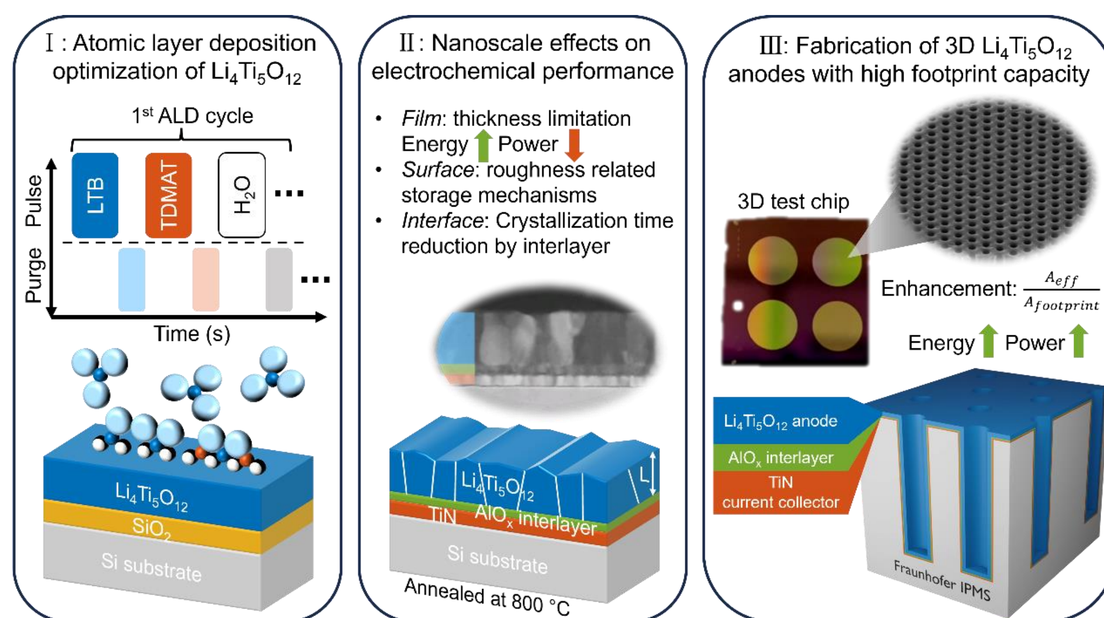

Figure 1. Overview of the proposed strategy for the fabrication of 3D LTO with high footprint capacity and rate capability and the required optimization steps.

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2.1. ALD Process Development of LTO

Spinel LTO thin films were successfully manufactured by developing a three-step ALD process with LTB, TDMAT, and deionized water (H_2O). In contrast to our previously published ALD process with LTB, all purge times were increased to 10 s, enabling a more reliable process, saturated GPC, and improved uniformity on 200 mm silicon substrates.[33] Furthermore, the ALD temperature window was investigated for the first time in this study. During process developments on thermal SiO_2 wafers, the LTB pulse time was varied while all other parameters were kept constant. In-situ spectroscopic ellipsometry (iSE) and scanning electron microscopy (SEM) were employed to determine the thickness of the dense, homogenous, and crack-free films. Overall, the thickness values extracted by both methods are in good agreement considering the error of 0.025 and 0.030 Å $cycle^{-1}$ for iSE and SEM, respectively. **Figure 2**a illustrates the GPC variation depending on the LTB pulse time for depositions with 500 cycles. Without LTB injection, TiO_2 is formed with a GPC of 0.45 Å $cycle^{-1}$. Increasing the LTB pulse time leads to higher GPC starting from 0.56 Å $cycle^{-1}$ at 2 s. Saturation of the ALD process occurs for a pulse time of 7 s with a GPC of 1.06 Å $cycle^{-1}$. A plateau is visible for extended LTB pulses with slightly increasing GPC up to 1.17 Å $cycle^{-1}$ for a 12 s pulse. The increase could be explained by precursor decomposition leading to partial CVD-like deposition.

The optimized GPC of 1.06 Å $cycle^{-1}$ is significantly higher than the 0.28 Å $cycle^{-1}$ for a 2.5 s LTB pulse reported in the previous work by Bönhardt et al.[33] The three-step ALD process with LiHMDS and TDMAT developed in our earlier study revealed an optimized GPC of 0.6 Å $cycle^{-1}$.[18] However, extended pulse times exhibit a GPC around 1.0 Å $cycle^{-1}$ but suffer from $Li_xSi_yO_z$ impurities originating from the Si inside precursor. Other reported ALD processes with LTB applied classic supercycles with different Ti:Li pulse ratios and Ti precursors to form LTO.[30,31] A saturated process with a 2:1 pulse ratio reached a GPC of 0.6 Å $cycle^{-1}$.[30] A combination of 5 Ti-O and subsequent 4 Li-O subcycles enabled a growth per supercycle of 5.5 Å $cycle^{-1}$.[31] The GPC, in an approximate conversion, is in good agreement with the ALD process developed here.

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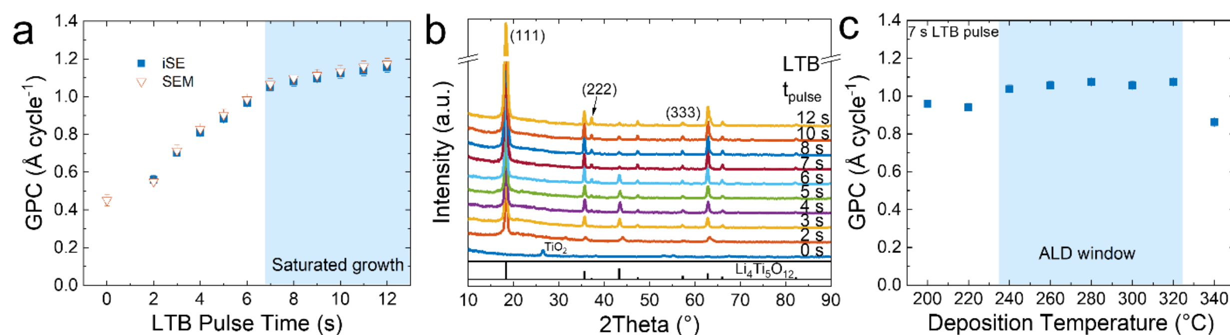

Figure 2. $Li_4Ti_5O_{12}$ ALD process development at 300 °C with LTB pulse time-dependent (a) GPC and (b) GI-XRD diffractograms with interrupted Y-axis after annealing. Pattern comparison performed with $Li_4Ti_5O_{12}$ (PDF 00-049-0207). (c) Deposition temperature-dependent GPC with a constant 7 s LTB pulse.

The morphology of the crystalline LTO films was probed by atomic force microscopy (AFM). The as-deposited amorphous samples were annealed at 700 °C for 30 s with rapid thermal processing (RTP). **Figure S1** shows the surface maps of the LTO films with various LTB pulse times after crystallization. The film with a saturated 7 s LTB pulse exhibits a root-mean-square (rms) value of 5.7 nm. Longer pulse times lead to a higher surface roughness of 9.1 and 13.4 nm for LTB pulses of 10 and 12 s, respectively. The rougher surfaces could be explained by the increased film thickness from 53.0 to 58.5 nm. Another factor could be the partial CVD-like deposition leading to precursor decomposition and non-uniform growth.

The phase information of the annealed LTO films was probed by grazing-incidence X-ray diffraction (GI-XRD). Figure 2b shows the 2θ diffractograms of the polycrystalline films with different LTB pulse times. The process without LTB results in the formation of TiO_2. All other films match spinel $Li_4Ti_5O_{12}$ (PDF 00-049-0207) with a cubic crystal system and Fd-3m spacegroup. Phase impurities were not visible in the GI-XRD analysis but cannot be excluded. However, here, the Si impurities are avoided by applying the LTB precursor. The comparison of the main (111) reflex of LTO around 18.33° for different LTB pulse times is displayed in **Figure S2**a. The peak height increases with LTB pulse time according to the thicker films. However, intensity growth in the saturated growth region could additionally be caused by an enlarged texture. In general, all LTO films demonstrate a strong (111) texture. It is noticeable that the LTO (400) reflex around 43.3° is visible up to a pulse time of 6 s. The films in the saturated growth region demonstrate a strong decrease in that peak height. However, the higher order peaks (222) and (333) around 37.20° and 57.30° become more visible. This shift

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of the peak intensities underlines the intensified (111) texture of the LTO films in the saturated ALD region.

The strong (111)-texture of the developed LTO thin films is in accordance with the previously reported LTO films based on a similar three-step ALD process with LiHMDS.[18] The weaker texture of the LTO fabricated by the initially published LTB process is probably related to the lower LTB dose and thickness compared to the films in this study. Overall, both Li precursors LTB and LiHMDS can be applied in an ALD process to achieve (111)-textured LTO films on thermal SiO_2 substrates. Other reported LTO films by ALD demonstrated weak (111)- or pronounced (400)-textures depending on the substrate.[30,31]

The temperature dependency of the deposition was investigated between 200 and 340 °C with a constant saturated 7 s LTB pulse. Figure 2c illustrates an ALD temperature window between 240 and 320 °C with a slight GPC variation between 1.04 and 1.08 Å $cycle^{-1}$. The GPC drops to 0.94 Å $cycle^{-1}$ at lower temperatures, indicating less reactivity. Furthermore, the deposition at 200 °C is only slightly higher than the temperature of the heated delivery lines (180 °C). The smaller difference between both temperatures could be more prone to cold spots inside the ALD chamber with precursor condensation. The GPC decreases at elevated deposition temperatures of 340 °C to 0.87 Å $cycle^{-1}$, which could be related to precursor desorption. The present study is the first investigation of the ALD temperature window with LTB for the fabrication of LTO. Except for 240 °C, the ALD window is in accordance with the process based on LiHMDS.[18] Both Li precursors offer a wide temperature range for stable LTO ALD processes. Furthermore, linearity and surface-inhibited growth are demonstrated for the developed ALD process, which is discussed in detail in the Supporting Information.

In summary, the developed ALD process with LTB to fabricate LTO thin films demonstrates all ALD characteristics, such as GPC saturation, temperature window, and linearity. Next, the influence of the substrate on the film crystallization is discussed.

2.2. Interface Engineering of LTO

A strong dependency of the crystallization and texture of ALD LTO on the substrate was discovered in our previous study.[18] The required annealing time and temperature for the complete crystallization of LTO is significantly increased on TiN compared to SiO_2 substrates. TiN is the optimal Si-technology-compatible current collector and Li diffusion

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barrier.[36] The several minutes longer high-temperature exposure can cause film delamination, impurity generation, Li loss, and increased surface roughness.[18,34] Another issue is potential oxygen diffusion through the TiN interface.[34] These factors can adversely affect the reproducibility of the annealing process, leading to inferior electrochemical properties of the LTO film. Furthermore, the prolonged annealing could impede the on-chip integration of 3D TFBs due to the thermal budget of other components. Hence, the objective is to reduce the required annealing time for the LTO crystallization on TiN. Several phenomena that could cause the inhibited crystal growth of LTO on TiN, such as differences in interface energies and thermal expansion coefficients, were already discussed.[18] Introducing a seed layer is one solution to decouple the LTO crystallization from the TiN interface. The interlayer can control the nucleation behavior, crystallization temperature, and induced film stress of the film above.[37–39] The influence of different interlayers on the phase and the optimum annealing temperature was demonstrated for HfO_2 thin films.[37,38] Hence, an amorphous AlO_x interlayer acting as a seed layer between the TiN and LTO is proposed and studied next.

The influence of amorphous AlO_x interlayers on the crystallization of LTO thin films was investigated by GI-XRD. All LTO films were manufactured with a 7 s LTB pulse and 500 ALD cycles. **Figure 3**a displays the LTO diffractograms with 100 nm thermal SiO_2 and 10 nm TiN substrates as references. The optimized RTP annealing procedure is 30 s at 700 °C on SiO_2 and 10 min at 750 °C on TiN. Higher crystallization temperatures lead to film delamination on TiN, similar to LTO thin films based on LiHMDS.[18,34] It is visible that the LTO reflexes on the SiO_2 substrate are sharper and more distinct compared to the TiN substrate. **Figure S3**a reveals that the LTO (111) reflex of the TiN sample exhibits a one-third lower peak height and is shifted to 18.43°. The peak difference of 0.1° compared to the SiO_2 substrate could be induced by compressive strain due to differences in the thermal expansion coefficient. Introducing an AlO_x interlayer with 100 ALD cycles on the TiN substrate significantly reduces the required annealing time and temperature to 30 s and 700 °C, as displayed in Figure 3a. These annealing parameters are identical to the SiO_2 substrate, although the LTO peaks are less distinct and the (111) peak height is lower. However, the strong (111)-texture of the LTO film, which is beneficial for the electrochemical performance, is not affected by the interlayer.[18] The peak shift is the same as for the TiN substrate without an interlayer, as displayed in Figure S3a. The (111) peak height is significantly higher than that on blank TiN substrates.

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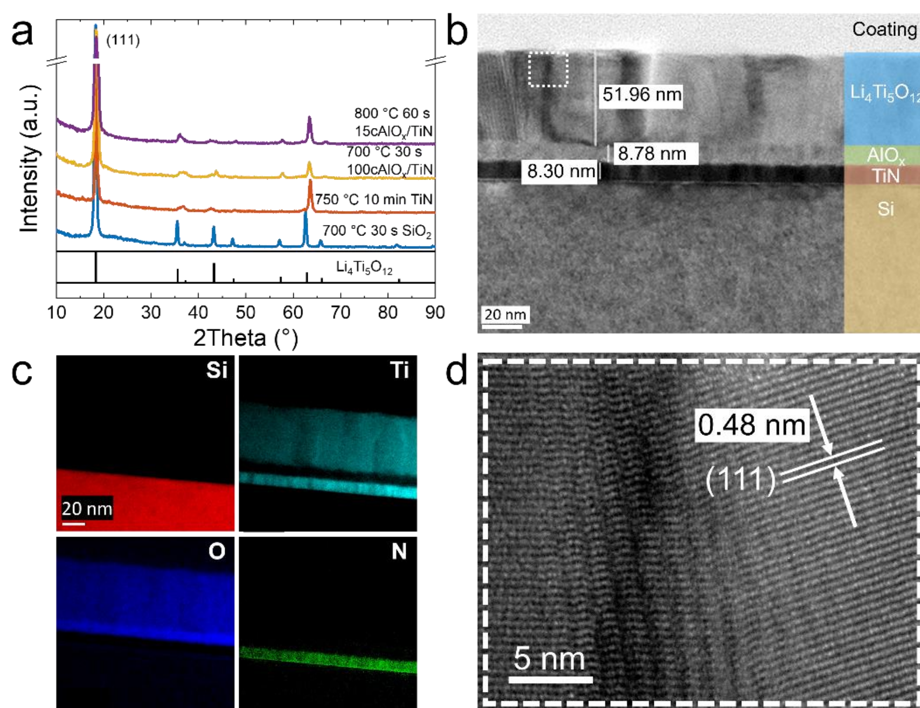

Figure 3. (a) GI-XRD diffractograms with interrupted Y-axis of LTO on various substrates and AlO_x interlayers with different annealing conditions. Pattern comparison performed with $Li_4Ti_5O_{12}$ (PDF 00-049-0207). (b) TEM micrograph and (c) EFTEM elemental maps for Si, Ti, O, and N of the layer stack with a 100-cycle AlO_x interlayer. (d) High-resolution TEM of LTO with a lattice spacing of 0.48 nm.

Structural and elemental characterization demonstrate that the AlO_x interlayer has sharp interfaces without visible intermixing. Figure 3b shows a transmission electron microscopy (TEM) micrograph of the annealed layer stack with an 8.78 nm thick AlO_x interlayer for 100 ALD cycles. Hence, the average GPC is 0.88 Å cycle^{-1}. The thickness of the TiN current collector is lower than expected at 8.3 nm, whereas the LTO is as estimated at around 52 nm. The amorphous nature of the AlO_x is visible in the brightfield TEM micrograph in Figure S3b. This is in accordance with the XRD diffractogram and a reported crystallization temperature of 850 °C for 60 s for an 8 nm thick Al_2O_3 film.[40] A qualitative comparison of the lateral crystallite size shows that the LTO crystallites are significantly larger than the TiN crystallites. The high-resolution TEM micrograph of the enlarged dashed area in Figure 3d confirms the spinel LTO with interlayer spacing of 0.48 nm matching (111) planes and a high crystallinity. The high interface quality is confirmed by energy-filtered TEM (EFTEM) elemental maps in Figure 3c. No interface mixing with the interlayer is visible since the Ti and N signals exhibit a sharp drop towards the AlO_x layer. The O signal is not visible in the area of the TiN layer and has a lower intensity within the LTO layer. The Al signal was not

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detectable without significant drift, but the EDX line scans discussed in the Supporting Information indicate no outdiffusion of Al.

After the successful proof of concept, the interlayer must be optimized towards electrical conductivity while maintaining the annealing time reduction. Sufficient conductivity can be achieved by reducing the thickness of the insulating AlO_x interlayer. Direct tunneling is observed for Al_2O_3 films fabricated by ALD with thicknesses of 3 nm and below.[41] The detailed examination of AlO_x interlayers with different thicknesses, elaborated in the Supporting Information, reveals that 15 cycles of AlO_x are the optimal interlayer for the electrochemical properties and crystallization time enhancement of LTO.

The proposed reduction of the required crystallization time and temperature of LTO by applying an ultrathin amorphous AlO_x interlayer was demonstrated for the first time. The effects agree with other reported interlayers for oxide materials.[37,39] However, the interlayer did not alter the phase or texture of the LTO film. Lacey et al. applied a 2 nm crystalline Al_2O_3 buffer layer to reduce the lattice mismatch for epitaxial growth of LTO on Si(111) substrates.[42] The thereby lowered growth temperature improved the crystallographic and electrochemical properties of the LTO film.

2.3. Electrochemical Performance of Planar Nanoscaled LTO

The effect of nanoscaling planar ALD LTO films on the electrochemical performance will be discussed next. Different film thicknesses of 25, 50, and 75 nm LTO were manufactured. Optimized LTO films with a 7 s LTB pulse time and a 15-cycle amorphous AlO_x interlayer were coated on 10 nm ALD TiN current collectors. All samples were annealed for 90 s at 800 °C to ensure full crystallization and electrochemical activity.

Figure 4 demonstrates that the LTO film thickness significantly affects the electrochemical behavior, especially at high C-rates. The cyclic voltammetry (CV) scans at 0.5 mV s^{-1} in Figure 4a show that all samples exhibit the characteristic LTO redox pair reaction around 1.55 V versus Li^+/Li. However, the peak separation and the maximum current increase with increasing film thickness. The 25 nm film reveals lithiation and delithiation peaks at 1.47 and 1.58 V versus Li^+/Li. The 50 and 75 nm films exhibit shifted peaks at 1.45 and 1.44 V versus Li^+/Li (lithiation) and 1.59 and 1.60 V versus Li^+/Li (delithiation). The current peaks are almost symmetric for all samples. The maximum footprint peak current increases with the

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film thickness from 33 to 45 and 60 µA cm^{-2}, respectively. Significant peak broadening occurs for the thicker films. Furthermore, non-peak currents are more prominent with increasing film thickness. The 75 nm LTO film exhibits extended non-peak currents of 10 µA cm^{-2} around 1.25 and 1.75 V versus Li^+/Li. The CV scans reveal increasing ionic and electronic resistance with the film thickness, which is apparent by the peak shifting and broadening. This behavior is as expected, assuming a constant resistivity value for the prepared LTO samples. However, the large non-peak currents are probably caused by a surface effect and will be further analyzed in the galvanostatic measurements next. In comparison, the 25 nm film shows similar peak shifting but significantly smaller peak currents than the 30 nm LTO film manufactured by ALD with a LiHMDS precursor from our previous study.[18] The lower peak current cannot only be explained by the reduced film thickness but could also indicate a lower film conductivity of the LTB-based LTO. Although both ALD LTO films demonstrated a beneficial (111)-texture, different degrees of parallel-oriented grains in the polycrystalline films could influence the electrochemical properties. According to Cunha et al., lithiation occurs first via the grain boundaries with subsequent radial insertion into the grain.[43] The in-plane crystallite size was not detectable for the comparison of the diffusion pathways length. Furthermore, the LTO films made with LiHMDS exhibited Si incorporation from the precursor, which can act as a dopant to facilitate the Li-ion and electron migration.[27,34,44]

The galvanostatic charge and discharge cycles at 1 C between 1 and 2.5 V versus Li^+/Li in Figure 4b confirm the behavior in the CV scans and demonstrate increasing footprint capacity with increasing film thickness. All samples show the characteristic potential plateaus around 1.55 V versus Li^+/Li. The extracted lithiation and delithiation capacities are in good agreement, indicating high Coulomb efficiency for all thicknesses. Similar to the voltammograms, the overpotentials increase with the film thickness. The flat voltage areas of the 25 nm sample are located around 1.51 and 1.53 V versus Li^+/Li for lithiation and delithiation. The thicker LTO films exhibit plateaus around 1.49 and 1.54 V versus Li^+/Li for 50 nm and 1.47 and 1.57 V versus Li^+/Li for 75 nm. The normalized galvanostatic profiles in **Figure S5**a elucidate the differences in the overpotentials. The plateaus of the 75 nm film have a noticeably steeper slope than thinner samples. This confirms the observations in the CV scans indicating higher resistance. Furthermore, the non-plateau capacities have a higher ratio for thicker films. The plateau capacities at 1 C exhibit ratios of around 80, 72, and 67 % for 25, 50, and 75 nm samples. The tails of the potential curves show a less steep decline

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above and below the plateaus with increasing film thickness. In previous studies, the non-plateau capacities were attributed to surface storage contributions.[18,43]

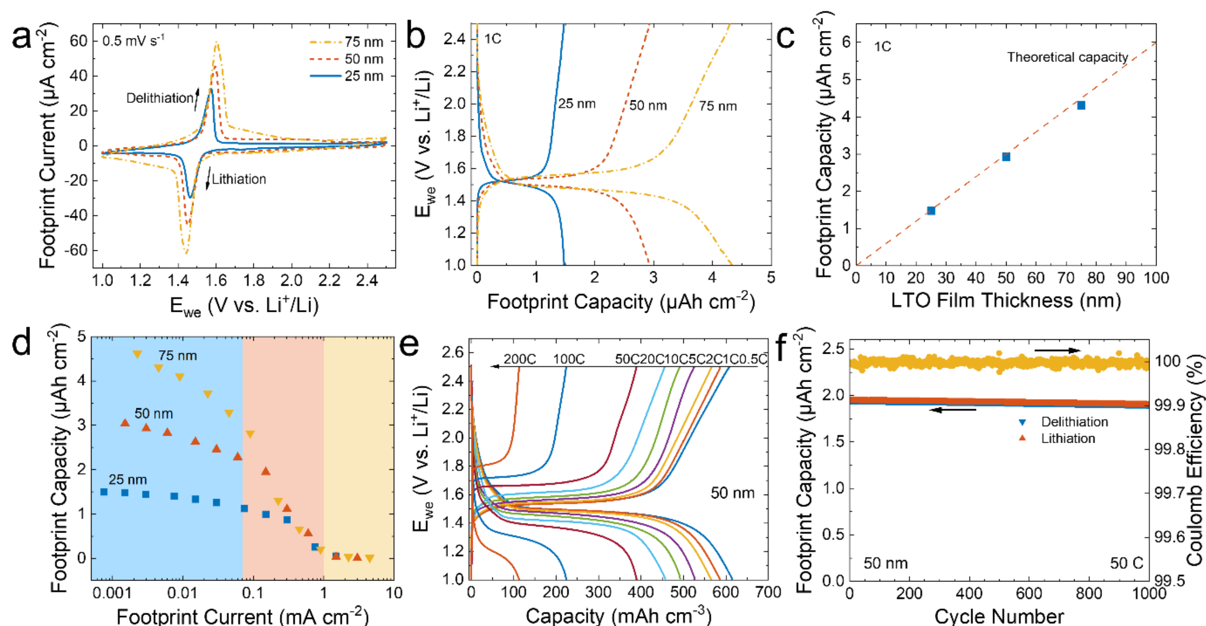

Figure 4. Film thickness dependence of (a) CV scans, (b) galvanostatic charge-discharge cycles, (c) the footprint capacity, and (d) the power performance. (e) Galvanostatic potential profiles at C-rates from 0.5 to 200 C and (f) long-term cyclability at 50 C for 1000 cycles of a 50 nm LTO film.

Overall, the more prominent surface capacities for thicker films contradict other studies.[43,45] Simulated voltage profiles by Ganapathy et al. predicted lower tail capacity ratios with increasing film thickness due to the higher bulk-to-surface ratio.[45] This behavior was confirmed experimentally for epitaxial LTO with different thicknesses.[42,43] The opposite dependency determined here could be related to the increasing surface roughness and possible higher amount of (111) and (110) surface facets, allowing additional storage.[18,43,45] The 75 nm LTO film exhibits a rms roughness of 13.9 nm in AFM surface maps, as displayed in **Figure S6**. This roughness is more than twice compared to 50 nm samples. The smoothest surface with a rms value of 2.6 nm was extracted for the 25 nm film. In contrast, the epitaxial LTO film showed smoother surfaces depending on the orientation with a minimal rms roughness of 1.4 nm for 220 nm films.[43] The ALD process could suffer from CVD-like deposition at later cycles due to the formation of hygroscopic LiOH on the colder chamber walls. This phenomenon could cause the rougher surface and lead to impurities for thicker LTO films, enhancing the surface storage contribution.

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Comparing the galvanostatic profiles with other LTO thin films, the bulk capacity relative to the film thickness is superior to non-ALD films. A slightly higher ratio of around 85 % and flatter plateaus were extracted for 30 nm ALD LTO films with LiHMDS in our previous study.[18] 20 nm epitaxial LTO films exhibited a lower bulk capacity, around 55 %.[46] A ratio of around 50 % was reported for epitaxial LTO in the range of 50 nm.[42,43] However, Lacey et al. reported the galvanostatic profiles at a high C-rate of 25 C with a large capacity of around 900 mAh cm^{-3}, exceeding the theoretical capacity (C_{th}) limit of 600 mAh cm^{-3} for LTO.[42] Typically, the surface capacities decrease with increasing C-rates.[18,42,43] The 90 nm epitaxial film exhibited a bulk capacity of 80 % at 3 C.[42] The effect of the film thickness on the overpotential is similar for epitaxial LTO films.[42]

Figure 4c illustrates that the delithiation footprint capacity linearly increases with the LTO film thickness. The capacities extracted at 1 C approximately follow the theoretical increase. It should be noted that at 0.5 C, the capacity of the 75 nm film exceeds the theoretical limit due to the higher surface capacity contribution discussed earlier. The delithiation footprint capacities at 1 C for 25, 50, and 75 nm LTO films are 1.48, 2.93, and 4.31 µAh cm^{-2}. The deviation from the theoretical values increases for thicker samples, for example a footprint capacity of 4.5 µAh cm^{-2} is expected for the 75 nm LTO. The higher difference could be related to the larger surface capacities.

The film thickness-dependent power performance illustrated in Figure 4d demonstrates that 50 nm LTO films are the optimal compromise of footprint capacity and current. The delithiation capacities were extracted at C-rates of 0.5 to 1000 C in the potential range of 1 to 2.5 V versus Li^+/Li. The absolute footprint currents are displayed to easily compare the accessible footprint capacity at relevant currents. The relation to the C-rate will be discussed in comparison with other LTO thin films later in this section. In general, three distinct regions are visible in Figure 4d. At low currents below 0.075 mA cm^{-2}, significant differences in the footprint capacities are apparent according to the film thickness. Between 0.075 and 1 mA cm^{-2}, the values converge. No significant capacities can be extracted for all planar films for currents above 1 mA cm^{-2}. The 25 nm film exhibits a plateau around 1.45 µAh cm^{-2} up to 0.0075 mA cm^{-2}. After a slight decrease, the capacity drops significantly at 0.75 mA cm-2 to 0.25 µAh cm^{-2}. The capacity of the 50 nm film exhibits a slight decline from 3.0 to 2.3 µAh cm^{-2} in the first region. A stronger decrease is visible at higher currents, with the highest reduction from 1.95 to 1.12 µAh cm^{-2} at 0.15 and 0.3 mA cm^{-2}, respectively. A

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significant capacity decline with a constant slope is observable for the 75 nm film up to 0.09 mA cm^{-2}. The initial footprint capacity of 4.6 µAh cm^{-2} decreases to 2.8 µAh cm^{-2}. In the second region, a drop of over 50 % to 1.3 µAh cm^{-2} at 0.24 mA cm^{-2} is apparent. From these footprint currents onward, the 50 nm exhibits the highest footprint capacities, demonstrating a superior power performance. Hence, 50 nm LTO films are selected for further evaluation on microstructured substrates in the following sections. The extracted thickness-dependency of the power performance is in accordance with experimental and simulated data of LTO films suggesting a limitation by Li-ion diffusion.[43]

The potential profiles of the 50 nm LTO ALD film at C-rates from 0.5 to 200 C in Figure 4e illustrate the large bulk capacities, even at extreme currents. The extracted lithiation and delithiation capacities are in good agreement, indicating high Coulomb efficiency over the whole C-rate range. All profiles show the characteristic potential plateaus around 1.55 V versus Li^+/Li. At low C-rates up to 2 C, the slope and position of the plateaus are very similar. The polarization and plateau shifting increase with higher C-rates. Starting from 50 C, the plateaus become asymmetric, with an increasing slope of the lithiation plateau, indicating higher lithiation resistance. The large capacity drop from 390 to 223 mAh cm^{-3} at 50 to 100 C matches the significant lithiation plateau shifting from 1.38 to 1.30 V versus Li^+/Li. The distinct delithiation plateau at 200 C demonstrates a dominant bulk intercalation ratio of around 85 %, resulting in a total capacity of 113 mAh cm^{-3}. Overall, the surface capacity contribution decreases significantly with the increase in C-rate. This behavior is in agreement with the LiHMDS-based ALD LTO film.[18]

Excellent long-term, high-rate cyclability at 50 C of the 50 nm ALD LTO film is demonstrated in Figure 4f. This C-rate, corresponding to a current of 0.15 mA cm^{-2}, was selected since it is the optimum energy and power density working point. The initial footprint capacity of 1.95 µAh cm^{-2} decreases to 1.90 µAh cm^{-2} with a high Coulomb efficiency of 99.9975 %. The exceptional capacity retention of 97.5 % after 1000 cycles demonstrates the highly reversible Li-ion insertion mechanism of the LTO thin film. Figure S5b illustrates that the potential profile after 1000 cycles is highly similar to the initial cycle indicating stable solid-electrolyte-interphase (SEI) and surface reconstruction. A similar capacity retention of 97.9 % after 1000 cycles at 100 C was reported previously for the 30 nm ALD LTO film with LiHMDS.[18] Evaluation of 50 nm epitaxial LTO film for 5000 cycles at 100 C revealed a capacity loss of only 9 %.[42] The superior cyclability could be related to the higher film

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quality of the epitaxial LTO. In general, LTO can achieve even better capacity retention of 99.5 % after 2000 cycles at 50 C for nanosheet-based hierarchical microspheres in standard electrode slurry applications.[47] However, thin films typically exhibit inferior stability due to film delamination and degradation.

The excellent C-rate performance of the evaluated ALD LTO is benchmarked against other planar LTO thin films in **Figure 5**. It should be noted that only the best-performing LTO films manufactured with various deposition techniques were considered for better visibility.[18,19,42,48,49] The comparison of the C-rate performance is challenging due to differences in the reported voltage range and subsequent inclusion or exclusion of the surface capacity. Applying a voltage window of 1.5 to 1.6 V versus Li^+/Li to extract the bulk delithiation capacity is sufficient for low C-rates but can be too narrow for high C-rates due to the polarization and significant plateau shifting. Nevertheless, trends can be extracted, and the illustration could help monitor the development of LTO thin films. The ALD LTO films have similar or superior bulk capacity ratios compared to other films.[18,19,42,48,49] Generally, the capacity retention at higher C-rates, predominantly above 50 C, benefits from scaling the film thickness down. The 25 nm ALD film with LTB, reported here, performs slightly better above 100 C than the 30 nm ALD film with LiHMDS.[18] Both ALD LTO films exhibit the electrochemically beneficial strong (111)-texture due to the (111) growth direction of the ALD TiN current collector.[18] The reduced thickness could compensate for the presumable lower conductivity of the ALD film with LTB discussed earlier. In the range of 5 to 50 C, the 50 nm film exhibits a similar performance as two times thicker films.[42,48] At 85 C, the sputtered film exceeds the capacity of the 50 nm ALD film at 100 C. The best C-rate performance was reported by Lacey et al. for an epitaxial 50 nm LTO film.[42] Capacities of 370 and 200 mAh cm^{-3} at extreme rates of 500 and 1000 C were achieved. It should be noted that large total capacities with a surface contribution of 45 % were revealed to exceed the theoretical bulk capacity limit by a factor of 1.5. In contrast, a significantly lower capacity was presented for the epitaxial 90 nm film by only considering the bulk capacity.[42] In general, non-epitaxial film are a superior choice for the fabrication of 3D TFBs due to the different surface orientations of microstructured substrates.

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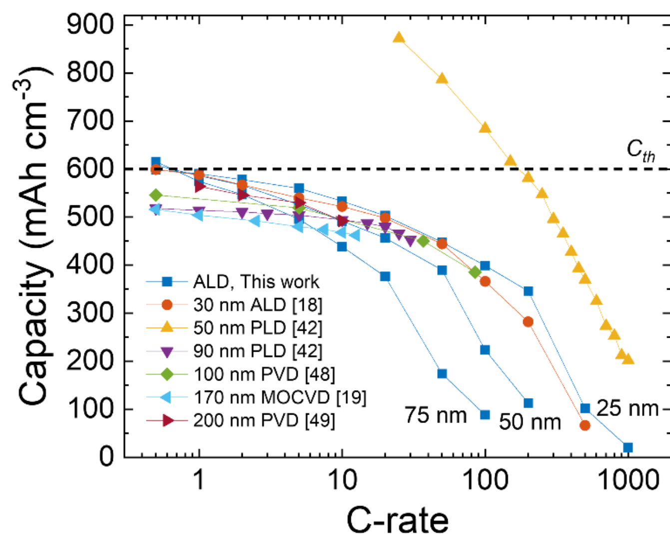

Figure 5. Comparison of the rate capability of the here developed ALD LTO films with other LTO thin films fabricated by various deposition techniques in recently reported studies. The capacities were estimated based on their results of the C-rate performance. The dashed line indicates the theoretical capacity (C_{th}) limit.

In conclusion, interface-engineered ALD LTO films demonstrated nanoscaling effects on the bulk capacity and electrochemical performance. The 50 nm film exhibits the best compromise of footprint capacity and current with an outstanding cyclability. Although, the developed ALD LTO films have excellent properties, the overall footprint capacity is too low for practical applications especially at high currents around 1 mA cm^{-2}. Hence, ALD LTO thin films coated on microstructured substrates will be investigated next.

2.4. Conformal ALD of LTO on Microstructured Substrates

The optimized ALD process with LTB for planar LTO films must be adapted for conformality in area-enhanced 3D Si substrates. Pre-tests revealed a inferior conformality of optimized LiHMDS-based LTO from our previous study compared to LTB, which agrees with other materials with these precursors.[18,35] In general, a higher dose of precursor molecules is required due to the increased surface area and longer diffusion time to the bottom of the HAR structures.[50] Also, longer purges allow the by-products to diffuse from the 3D structures. Hence, LTO ALD processes with longer LTB pulse and purge times were carried out. A 3D test chip was Si-technology compatible fabricated via electron beam lithography and reactive ion etching.[36] Hexagonal arrays of holes with aspect ratios of 10:1 and 20:1 were employed

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as conformality 3D test structures. **Figure S7** exemplary shows the 10:1 structures with a hole diameter of around 0.81 µm and a depth of 8.3 µm. The substrates were first coated by ALD with 8 nm TiN. Details of the TiN deposition with a conformality of around 100 % can be found in an earlier publication.[36]

An LTO ALD process with 11 s pulse and 20 s purge steps of LTB demonstrated the best step coverage of around 70 % for structures with an aspect ratio of 10:1. The purge time was the key factor for a conformal coating of LTO. **Figure 6** shows the SEM micrographs with a total thickness of the TiN/LTO layer stack of 41.4 and 30.9 nm at the top and bottom of the holes, respectively. It should be noted that the LTO and TiN films are not distinguishable within the holes. Hence, the assumed thickness of 8 nm for TiN is subtracted to obtain the LTO thickness. The GPC at the top surface of 1.11 Å $cycle^{-1}$ is slightly lower than for the planar ALD process with 1.16 Å $cycle^{-1}$. The extended purging of 20 s compared to 10 s could lead to the desorption of surface species.[9] The discussion of the influence of the process parameters on the conformality is conducted in the Supporting Information.

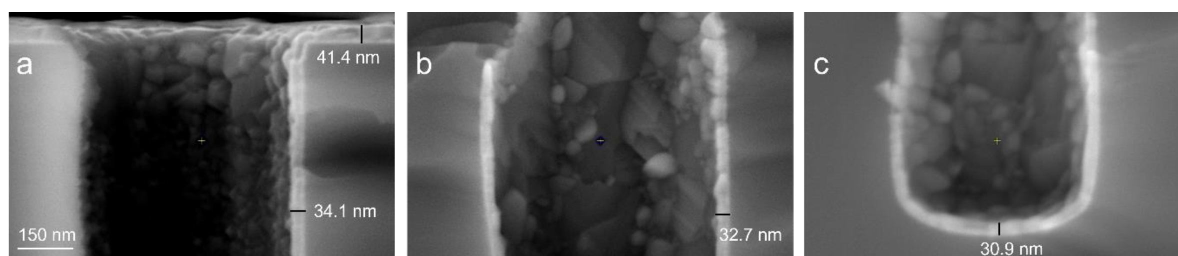

Figure 6. Cross-section SEM micrographs of the (a) top, (b) middle, and (c) bottom of structures with an aspect ratio of 10:1 for conformality tests of the optimized LTO ALD process.

The conformality of 70 % of the developed LTO ALD process with LTB is lower than that of the previously reported process with 85 % for 12:1 HAR structures.[33] However, the process by Bönhardt et al. showed a significantly lower GPC of 0.28 Å $cycle^{-1}$. This is close to the GPC of 0.45 Å $cycle^{-1}$ for the pure TiO_2 process. Hence, the distinction between the formation of LTO and TiO_2 inside the HAR structures by measuring film thickness is difficult. In general, evaluating the film stoichiometry inside HAR structures is highly challenging. In future studies, lateral HAR structures could be employed to investigate potential composition variations.[50,51] Furthermore, the LTO films in the previous study were not electrochemically investigated to exclude TiO_2 formation.[33] An inferior conformality of LTO manufactured by

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MOCVD was reported by Xie et al. with step coverage of 23 and 10 % for structures with aspect ratios of 1:1 and 3:1, respectively.[19]

Conformality assessment of other reported ALD processes with Li precursors demonstrated excellent results depending on the precursors and process. Lethien et al. presented LMO and LiPO films with conformalities close to 100 % for microtube pillar structures with aspect ratios of up to 80:1.[15,16] However, it should be noted that the equivalent aspect ratio of pillar structures compared to microholes is lower by a factor of three since the equivalent aspect ratio considers the ease of coatability.[50] The LMO film was fabricated by annealing a dual-layer stack of MnO_2 and LiOH.[15] The LTB-based LMO process was examined for structures with an aspect ratio of up to 33:1. The excellent conformality of LiPO was enabled by an ALD process with LTB and trimethyl phosphate in 80:1 HAR structures.[16] LiPON films manufactured by plasma-enhanced ALD with LTB demonstrated a conformality of 78 % for pillars with an aspect ratio 25:1.[52] A thermal ALD process with LTB and diethyl phosphoramidate resulted in LiPON films with a conformality of 95 % for holes with an aspect ratio of 10:1.[7] ALD processes without H_2O as the oxidant have the potential of higher conformality by avoiding the "water reservoir effect".[32] The 3-step ALD process applied here based on the steric hindrance of the adsorbed precursor species might be more prone to insufficient precursor diffusion and local partial pressure differences in the HAR structures.

In general, new Li precursors with higher reactivity resulting in higher sticking probability and higher thermal stability leading to minimal CVD-like deposition should be developed for the mass production of 3D TFBs. Next, the developed LTO films on microstructured substrates will be electrochemically investigated.

2.5. Electrochemical Analysis of High-Capacity 3D LTO

For the first time, 3D LTO anodes fabricated by ALD were electrochemically evaluated. The analysis of 3D LTO demonstrates a significant footprint capacity improvement while maintaining high power performance and cyclability. The optimized ALD process was employed to manufacture 50 nm LTO films on TiN-coated microstructured p-type Si substrates with a 15-cycle amorphous AlO_x interlayer. According to the planar samples, annealing was conducted for 90 s at 800 °C for full crystallization and electrochemical activity. The hexagonal hole arrays introduced in the previous section with aspect ratios of 5:1

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and 10:1 result in AEFs of 5 and 9. Hereafter, the 3D LTO samples with AEFs of 5 and 9 will be referred to as AEF5 and AEF9 for better readability.

The area-enhancement effect is visible in **Figure 7**a by increasing peak heights of the CV scans at 0.5 mV s^{-1}. The peak currents are enhanced from 45 µA cm^{-2} for the planar LTO to 149 and 251 µA cm^{-2} for AEF5 and AEF9, respectively. A smaller peak separation of 0.12 V of the characteristic redox pair reaction is observable for 3D LTO, with lithiation occurring around 1.46 V versus Li^+/Li and delithiation around 1.58 V versus Li^+/Li, compared to 0.14 V for the planar sample. The CV scans do not reveal peaks related to TiO_2, indicating homogenous LTO stoichiometry without TiO_2 formation in the HAR structures. The broad non-peak currents attributed to surface reactions are significantly higher for 3D LTO than the planar sample, corresponding to the higher surface area.

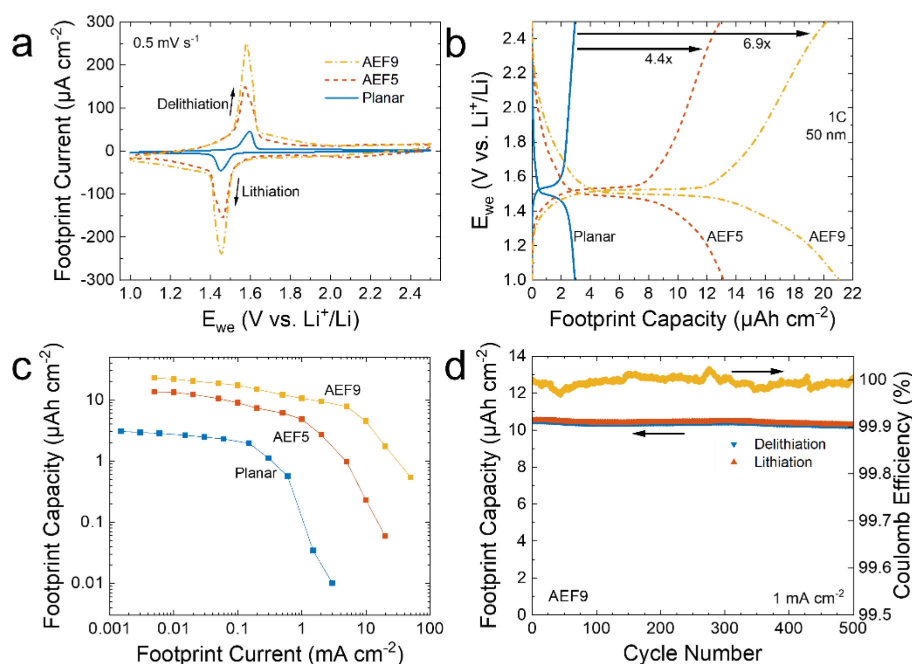

Figure 7. AEF dependence of (a) CV scans, (b) Galvanostatic charge-discharge cycles, and (c) the footprint power performance for 50 nm LTO films. (d) Long-term cyclability at 1 mA cm^{-2} for 500 cycles of 3D LTO with an AEF of 9.

The footprint capacity of 3D LTO is successfully increased by the area-enhanced substrates. Figure 7b illustrates the Galvanostatic charge and discharge cycles at 1 C between 1 and 2.5 V versus Li^+/Li of planar and 3D LTO. All LTO films exhibit the characteristic potential plateaus around 1.55 V versus Li^+/Li without indications of TiO_2. The potential plateaus of AEF5 and AEF9 are located at 1.49 and 1.50 V versus Li^+/Li (lithiation) and 1.53 and 1.52 V

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versus Li^+/Li (delithiation). The normalized potential profiles in **Figure S8**a illustrate that the polarization decreases with increasing area enhancement from 25 to 15 mV for planar and AEF9, respectively, and is consistent with the cyclovoltagrams. The lower polarization could indicate a superior conductivity of the 3D samples due to the decreased LTO film thickness by the non-conformal coating or grain size variations. AEF5 demonstrates a delithiation footprint capacity of 12.91 µAh cm^{-2}, which is an enhancement by a factor of 4.4 to the planar LTO. A further increase is reached for AEF9 with a remarkable footprint capacity of 20.23 µAh cm^{-2} at 1 C, representing a 6.9 times improvement. The only report on 3D LTO so far was by Xie et al. with around 21.9 µAh cm^{-2} at 0.2 C.[19] However, the enhancement was only 2.5 compared to the 170 nm planar film despite an AEF of 7.4 due to the insufficient conformality of the MOCVD process.

Both 3D LTO footprint capacities are below the theoretical increase expected by the AEF, as illustrated in Figure S8b. AEF5 and AEF9 attain around 88 and 77 % of the expected increase. The capacity deviation can be explained by the non-ideal conformality of the ALD process. For example, a step coverage of 70 % was achieved in the 10:1 HAR structures, resulting in an AEF of 9. It should be noted that the average film thickness inside the HAR structure is approximately 75 % of the planar film after the thickness drop at the opening observable in Figure 6. The remaining capacity difference could be related to the thinner LTO reaching a higher amount of C_{th} or fluctuations in the aspect ratio. Another important factor could be the contribution of surface storage. Figure S8a illustrates the significant difference in the normalized potential profiles for planar and 3D LTO at 1 C. The 3D samples have a similar shape and exhibit a higher ratio of surface capacities than planar LTO. The bulk capacity ratio of 3D LTO is around 60 % compared to 72 % for the planar 50 nm LTO film. Similar to planar LTO films, the higher surface capacity ratios of 3D LTO could be related to an increased surface roughness. The 3D ALD process employs longer LTB pulse times, which can cause rougher surfaces due to a CVD-like growth as described in Section 2.1.

The excellent high-power performance of 3D LTO fabricated by ALD is demonstrated in Figure 7c. The maximum footprint capacity of 22.8 µAh cm^{-2} is achieved at 0.005 mA cm^{-2} (0.25 C) for AEF9. It should be noted that the capacity increase compared to 1 C is mainly attributed to the surface capacity. The highest footprint capacity of AEF5 is 13.6 µAh cm^{-2}. Up to 0.1 mA cm^{-2}, the obtained capacities are quite stable, with 17.4 (AEF9) and 8.9 µAh cm^{-2} (AEF5). The initial footprint capacity enhancement to planar films increases drastically

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for footprint currents above 0.5 mA cm^{-2} with increasing AEF. However, the effective C-rate at a fixed current is smaller for the 3D samples. At 0.5 mA cm^{-2}, remarkable footprint capacities of 12.1 and 6.1 µAh cm^{-2} are reached for AEF9 and AEF5. This is an enhancement of a factor of 21.6 and 10.9 compared to planar LTO. The deviation between the 3D samples becomes more significant for elevated currents. A 7.75 times higher footprint capacity is extracted for AEF9 at 5 mA cm^{-2}. At an extreme current of 10 mA cm^{-2}, AEF9 still exhibits 22 % of the capacity at 1 C with 4.46 µAh cm^{-2}. The rate performance of 3D LTO by ALD indicates that the lost total footprint capacity by the non-ideal conformality is partially compensated at extreme C-rates due to the consequent lower film thickness. The rate capability of 3D LTO fabricated by MOCVD has not been reported.[19] Hence, a benchmark with other 3D thin film anode materials will be conducted in the next section.

The outstanding high-current cyclability of AEF9 is displayed in Figure 7d. The initial footprint capacity at 1 mA cm^{-2} (50 C) of 10.52 µAh cm^{-2} decreases to 10.26 µAh cm^{-2} after 500 cycles. The high average Coulomb efficiency of 99.9951 % results in an excellent capacity retention of 97.4 %. The fluctuation of the Coulomb efficiency is slightly higher compared to planar LTO and could be related to the enlarged surface and its capacity contribution. Highly similar potential profiles of the first and last cycle in Figure S8c illustrate the stable lithiation mechanism of ALD LTO on 3D substrates. Furthermore, the high capacity retention indicates that SEI formation occurs without clogging the HAR structures. 3D LTO by MOCVD showed good cyclability over 160 cycles.[19] The slight initial increase of the first 100 cycles was explained by incomplete wetting due to the remaining gas at the bottom of the HAR structures. Generally, excellent cycle stability can be achieved for the most studied 3D anode TiO_2.[20,21,53] Moitzheim et al. demonstrated an average Coulomb efficiency of 99.96 % for 1000 cycles at 10 C.[21] The HAR structures with a higher AEF of 21 could influence the inferior cyclability compared to 3D LTO with a lower AEF employed here. The 3D SnN_x by Pearse et al. exhibited significantly lower capacity retention with a decrease of around 15 % for the last 80 cycles after a strong initial 25 % drop for the first 20 cycles.[7]

The first ever electrochemical investigation of 3D LTO by ALD reveals a footprint capacity enhancement of up to 6.9 at 1 C according to the AEF and the coating conformality. The combination of high capacity and high power is successfully demonstrated with 7.75 µAh cm^{-2} at 5 mA cm^{-2} (250 C). Excellent high-rate cyclability with a capacity retention of 97.4 %

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after 500 cycles at 1 mA cm^{-2} is achieved for ALD LTO with an AEF of 9. Next, the performance comparison to other 3D anode materials will be evaluated.

2.6. Benchmarking of 3D TFB Anodes

The 3D LTO with an AEF of 9 fabricated by ALD demonstrated an excellent high-power performance while maintaining high footprint capacities. Due to the lack of reported C-rate capabilities of 3D LTO, the benchmarking will be conducted with other 3D anode materials.[7,16,19–22,53] Only thin films on microstructured Si substrates are considered for the prospective realization of on-chip 3D TFBs. Generally, the benchmark is affected by various parameters such as different materials, AEFs, film thicknesses, and HAR structures. For example, micropillars facilitate the wetting of the liquid electrolyte due to larger spacings than in microholes. It should be noted that SnN_x is the only anode evaluated in a full-cell 3D TFB.[7] However, illustrating the footprint capacity versus the C-rate could act as a fair assessment for the orientation in further studies.

A superior C-rate performance above 50 C of 3D LTO by ALD is illustrated in **Figure 8**. 3D anodes with higher AEF and thicker films exhibit larger footprint capacities. Letiche et al. demonstrated the highest footprint capacity of 370 µAh cm^{-2} at C/16 by coating a 155 nm anatase TiO_2 film on a microstructured substrate with an AEF of 53.[16] Another high footprint capacity was achieved by the same group with 220 µAh cm^{-2} at C/12 for 150 nm anatase TiO_2 with an AEF of 25.[22] However, both 3D TiO_2 suffer from insufficient C-rate performances with significant drops to 20 % at 2 C (AEF 53) and 12 % at 4 C(AEF 25).[16,22] The best C-rate performance for TiO_2 was achieved by Moitzheim et al. by employing Cl-doped amorphous films.[20,21] The 100 nm films were coated by ALD and spatial ALD on HAR structures with an AEF of 21. 80 % of the maximum capacity of 242 µAh cm^{-2} was demonstrated at 2 C and 37 % at a high rate of 20 C. 10 nm SnN_x films with an AEF 10 exhibited similar footprint capacities as the presented 3D LTO with 13.5 µAh cm^{-2} at 11 C.[7] However, the maximum capacity was reported at 27 µAh cm^{-2} at 3.7 C. Around 22 % of the maximum capacity was achieved at a high rate of 75 C. The most significant advantage of 3D LTO over SnN_x is visible at 250 C with 8.2 µAh cm^{-2} compared to around 4 µAh cm^{-2} at 185 C. Overall, the 3D LTO by ALD showed superior relative capacities at high C-rates, with 55 % at 25 C, 38 % at 250 C, and 21 % at 500 C. It should be noted that the footprint capacity of 89 µAh cm^{-2} of thick TiO_2 films with high AEF at an absolute current of around 60 mA cm^{-2} is magnitudes of order larger than for 3D LTO with 0.54 µAh cm^{-2} at 50 mA cm^{-2}.[20,21]

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However, considering the extreme rate capability of planar ALD LTO films, this benchmark demonstrates the enormous prospective potential of 3D LTO by increasing the film thickness, AEFs, and conformality to manufacture high-energy and high-power 3D TFBs.

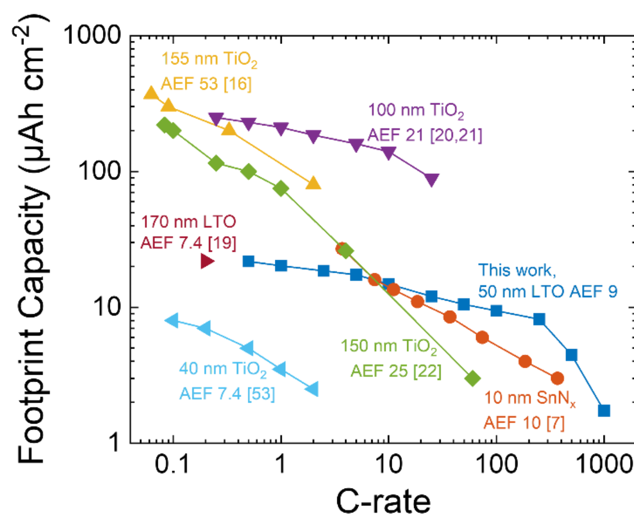

Figure 8. Comparison of the rate capability of 3D LTO by ALD with other 3D anode thin-film materials with various AEFs. The capacities were estimated based on their results of the C-rate performance.

3. Conclusion

In this study, interface-engineered LTO thin films fabricated by ALD on area-enhanced 3D substrates have been electrochemically evaluated for the first time, demonstrating high footprint capacities and excellent high-power performance with outstanding cyclability. The developed thermal ALD process with a LTB precursor and a GPC of 1.06 Å cycle^{-1} at 300 °C facilitates high-quality spinel (111)-textured LTO. Extended LTB pulse and purge times enable sufficient conformality on microstructured substrates with aspect ratios of up to 20:1. A technological breakthrough of significant annealing time reduction was achieved by introducing an ultrathin amorphous AlO_x interlayer to decouple LTO from the crystallization impeding TiN current collector interface. This interface-engineering approach could be extended to other battery materials requiring high-temperature crystallization to improve the integration with Si technology. Two routes for enhancing the footprint capacity of ALD LTO were explored. Increasing the planar film thickness from 25 to 75 nm enables capacities of 4.3 µAh cm^{-2} at 1 C and reveals nanoscale effects. Counterintuitively, thicker films lead to an enhancement of surface-type storage which could be explained by surface roughening. The C-rate performance improves with scaling down the LTO film thickness. However, 50 nm LTO reveals the best compromise of footprint capacity and rate capability and an excellent capacity

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retention of 97.5 % after 1000 cycles. We demonstrated a significant footprint capacity enhancement of 6.9 for 3D LTO with an AEF of 9 with a remarkable footprint capacity of 20.23 µAh cm^{-2} at 1 C. The outstanding high-power capability is confirmed with 7.75 µAh cm^{-2} at 5 mA cm^{-2} while preserving excellent high-rate cyclability. The superior performance of interface-engineered ALD 3D LTO at extreme rates above 50 C compared to other 3D anode materials paves the way for the required high-energy and high-power on-chip 3D TFBs for energy-autonomous mm-scale IoT devices.

4. Experimental Section

$Li_4Ti_5O_{12}$ sample preparation: $Li_4Ti_5O_{12}$ thin films were fabricated using ALD on a FlexAl system (Oxford Instruments) on 200 mm Si substrates. The reactor wall temperature was set at 150 °C to minimize precursor condensation. The ALD processes were carried out at a pressure of 80 mTorr. LTB (STREM Chemicals, >98%), TDMAT (Dockweiler Chemicals, electronic grade), and deionized water as an oxidant were applied. The LTB and TDMAT precursors were kept at 140 and 60 °C, respectively. Ar was used as the carrier and purge gas in heated lines to avoid condensation. A "soft draw" was utilized for LTB to minimize particle generation in the lines and the reactor. The procedure was described in a previous publication.[33] Here, the fill step was increased to 2 s to enable LTB pulse times between 0 and 12 s. TDMAT was used in bubbling mode. The pulse times of TDMAT and H_2O were set at 0.5 and 0.25 s, respectively. All purge steps were carried out for 10 s in case of the planar ALD process. The deposition procedure is based on the three-step ALD process to suppress the so-called "water reservoir effect" by minimizing the formation of hygroscopic LiOH. The novel concept is the introduction of a co-precursor step B (here TDMAT) between the LTB (A) and the H_2O (C) steps. Classic supercycle ALD processes consist of alternating subcycles with the basic order AC and BC. Details of this process were reported previously.[18,33] The substrate temperature was varied between 200 and 340 °C to investigate the ALD temperature window.

ALD process development was carried out on 200 mm Si substrates with 100 nm thermal SiO_2. Deposition of LTO for electrochemical characterization was performed on coupons from p-type 300 mm Si (100) substrates with a resistivity of 0.013 Ohm cm coated with 10 nm ALD TiN. The excellent Li-ion diffusion barrier performance and process conditions of the ALD TiN was reported previously. [36] Area-enhanced p-type 300 mm Si (100) substrates were applied for conformality and electrochemical characterization of 3D LTO

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samples. Details of the 3D test chip manufactured via electron beam lithography and reactive ion etching were published elsewhere.[36] The design offers various circular areas with 7 mm diameter comprising hexagonal arrays of holes with aspect ratios of either 5:1, 10:1, or 20:1. The hole diameters of 2, 1, or 0.5 µm and the constant depth of 10 µm result in AEF of 5, 9, and 17, respectively. The crystallization of all post-deposition amorphous LTO films was conducted in an Solaris 75 rapid thermal processor (SSI) with Ar purging.

Structural Characterization: Phase and crystallization information were obtained by GI-XRD analysis on a D8 Discover system (Bruker). Cu Kα radiation ($\lambda = 1.5406$ Å), 40 kV, and 40 mA were applied at an incidence angle of 0.3° with a 2θ range of 10 to 90°. The step time and size were set at 10 s and 0.1°, if not otherwise noted. Phi was set at 45° to suppress peaks related to the Si substrate. The ALD process was monitored by in-situ SE on a M2000X-210 (J.A. Woollam) in the wavelength range from 210 to 1000 nm and Xenon light source to obtain the growth per cycle. Tauc-Lorentz and Lorentz oscillators were applied in the dispersion model for fitting of the film thickness and the optical parameters. The surface morphology was probed by AFM on an Asylum Research Cypher S (Oxford Instruments). The film thickness, microstructure and conformality of the samples was observed by SEM on an ApreoS (ThermoFisher Scientific) and a S-5000 (Hitachi). TEM was carried out with an electron beam energy of 200 keV on a Tecnai F20 XT (FEI). The EDX elemental line scans were acquired in the scanning TEM (STEM) mode with a high-angle annular dark-field imaging (HAADF) detector. EFTEM using an imaging filter (Gatan) provided element-sensitive micrographs. Filter energies of 99, 402, 456, and 532 eV were applied for Si, N, Ti, and O, respectively.

Electrochemical Measurements: The electrochemical analyses were carried out in a three-electrode setup. 15 by 15 mm coupons of the $Li_4Ti_5O_{12}$ thin films on planar and 3D TiN substrates were employed for electrochemical examination. It should be noted that the samples were exposed to air after deposition and annealing, although it was kept to a minimum. TSC surface cells (rhd instruments) with an active area of 0.273 cm^2 were mounted in an argon-filled glovebox (Mbraun, H_2O and O_2 levels below 1 ppm). A 1M solution of lithium hexafluorophosphate ($LiPF_6$) in ethylene carbonate/diethyl carbonate (EC/DEC 1:1) (Sigma-Aldrich, battery grade) was employed as electrolyte. The cell was assembled with LTO thin film as the working electrode and Li stripes (Sigma-Aldrich, 99.9%) acting as counter and reference electrodes. The samples were contacted via the backside of the TiN-

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coated Si substrate. All electrochemical measurements were performed and analyzed with a SP-150 (Bio-Logic) and EC-Lab software. All potentials mentioned in this report were measured against Li^+/Li. The electrochemical measurements were performed in the potential range of 1 to 2.5 V versus Li^+/Li. A maximum theoretical volumetric capacity of 600 mAh cm^{-3} is considered. The C-rates are derived from the theoretical capacity according to the film thickness if not otherwise noted.

Supporting Information

Supporting Information is available online or from the author.

Acknowledgements

The authors would like to thank Kati Biedermann and Katrin Zimmermann for TEM, SEM, and AFM measurements. This work was supported by the German Federal Ministry for Economic Affairs and Climate Action (No. 03EN1036A).

Received: ((will be filled in by the editorial staff))

Revised: ((will be filled in by the editorial staff))

Published online: ((will be filled in by the editorial staff))

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