

# Non-volatile resistive switching in nanoscaled elemental tellurium by vapor transport deposition on gold

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## **ABSTRACT**

Two-dimensional (2D) materials are highly promising as resistive switching materials for neuromorphic and in-memory computing owing to their fascinating properties derived from their low thickness. However, most of the reported 2D resistive switching materials struggle with

complex growth methods or limited growth area. Tellurium, a novel member of single-element 2D materials, is showing pioneering characteristics such as simplicity in chemistry, structure, and synthesis which make it highly suitable for various applications. This study presents the first memristor design based on nanoscaled elemental tellurium synthesized by vapor transport deposition (VTD) method at a temperature as low as 100 °C in full compliance with a back-end-of-line (BEOL) processing. We demonstrate that the memristive behavior of nanoscaled tellurium can be enhanced by selecting gold as the substrate material which results in a lower set voltage and reduced energy consumption. In addition, the formation of conductive paths which in turn lead to resistive switching behavior on the gold substrate is proven to be driven by the gold-tellurium interface reconfiguration during the VTD process as revealed by energy electron loss spectroscopy analysis of the interface. Our findings reveal the potential of nanoscaled tellurium as a versatile and scalable material for neuromorphic computing systems as well as the influential role of gold as electrode material in enhancing tellurium's memristive performance.

## **INTRODUCTION.**

The rapid development of information and communication technologies is reshaping the way we interact with our surrounding environment. Notably, the effective management of big data is becoming increasingly important to navigate the complexities of our ever-changing environment. Despite the evident benefits derived from technological progress, significant challenges still exist that require advanced solutions in terms of newly engineered materials and operational paradigms. In this context, the demand for reducing power consumption has emerged as an urgent requirement for improving the efficiency and processing speed of electronic devices and systems. Traditional computing systems based on the von Neumann architecture that rely on the separation of memory

and central processing unit <sup>1</sup>, are incapable of fulfilling the performance demands of future technologies. As a response to this challenge, bio-inspired approaches, drawing inspiration from the structure of the human brain, such as neuromorphic architectures, have gained popularity <sup>2</sup>. Innovative designs emulating biological systems demonstrate the ability to simultaneously process large volumes of data while requiring minimal power consumption. In this context, resistive switching (RS) phenomena is emerging to implement the artificial synapses as a building block of a neuro-inspired computational architecture, that is capable of storing and processing data in a single device <sup>3</sup>. Briefly, the RS phenomena is characterized by cyclic changes in electrical resistivity between two distinct levels: high resistance state (HRS) and low resistance state (LRS) <sup>4</sup>. Non-volatile RS enables the state of the system to be retained without requiring a constant power supply. The RS effect can be observed in a wide range of materials with strong implications for memory applications, such as resistive random-access memories (RAM) or memristors. A memristor is a non-volatile memory device that was mathematically predicted as the missing fourth circuit element (besides the resistor, capacitor, and inductor) by Chua <sup>5</sup> in 1971 and experimentally demonstrated by Williams in Hewlett-Packard Laboratories in 2008 <sup>6</sup>.

The physical origins of the RS phenomenon vary significantly depending on the materials employed and device architectures. They include conductive filament formation <sup>7</sup>, crystallographic phase change <sup>8</sup>, charge trapping/de-trapping <sup>9</sup>, ferroelectric and magnetic <sup>10,11</sup>, spin- and photo-induced <sup>12,13</sup> switching mechanisms. Engineering the active material inside the memristive cell is a valuable strategy to substantially reduce the switching energy (and hence, the dissipated power) and time no matter the nature of the RS mechanism.

Various materials have traditionally demonstrated their implication in memristive devices including oxides. <sup>14</sup> In particular, metal oxides are taken as constitutive building blocks for

resistive switch RAM (so-called ReRAM) where the memristive behavior is dictated by voltage-induced effects like conductive filament formation, defect migration, ionic charge trapping, etc.

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In the ReRAMs framework, two-dimensional (2D) materials have recently attracted interest in memristive applications as they can concomitantly offer superior performance and flexibility.<sup>18,19</sup> Reducing the material thickness, down to the 2D limit bears potential advantages in neuromorphic computing in terms of fast and low-power switching, gate tunability and mechanical robustness for flexible electronic applications<sup>18</sup>. Recently, a wide range of 2D materials such as hexagonal boron nitride (h-BN)<sup>20–22</sup>, transition metal dichalcogenides (TMDs)<sup>23</sup> and TMDs heterostructures<sup>24,25</sup> have been employed for the development of memristor devices. Among 2D materials, the use of monoelementals has emerged due to the simplification in the compositional chemistry and the higher homogeneity at the nanometre scale out of adventitious bonding defects (vacancies, antisite defects, etc.) in nanoscale compounds. These features are expected to hinder the performance variations observed in materials with a more complicated chemical composition typically used in RS schemes.<sup>26</sup> Nonetheless, the consideration of elemental materials for memristor applications was limited to the case of black phosphorous (BP)/HfO<sub>x</sub> bilayer as artificial synapsis,<sup>27</sup> and no other alternative materials have been taken into account. One of the most recently discovered monoelemental 2D materials is tellurene, classified within the Xenes family<sup>28,29</sup>, and it is composed of covalently bonded tellurium atoms in helical chains connected by van der Waals forces.<sup>30</sup> After Zhu et al. experimentally verified tellurene in 2017<sup>31</sup>, numerous studies have been conducted as its follow-up.<sup>30,32–35</sup> Tellurene exhibits a semiconducting character with a thickness-dependent bandgap ranging from 0.3 eV in bulk up to 1.0 eV in the monolayer regime.<sup>36</sup> Tellurene research is mostly focused on its potential applications in optoelectronics and electrical devices<sup>37</sup>,

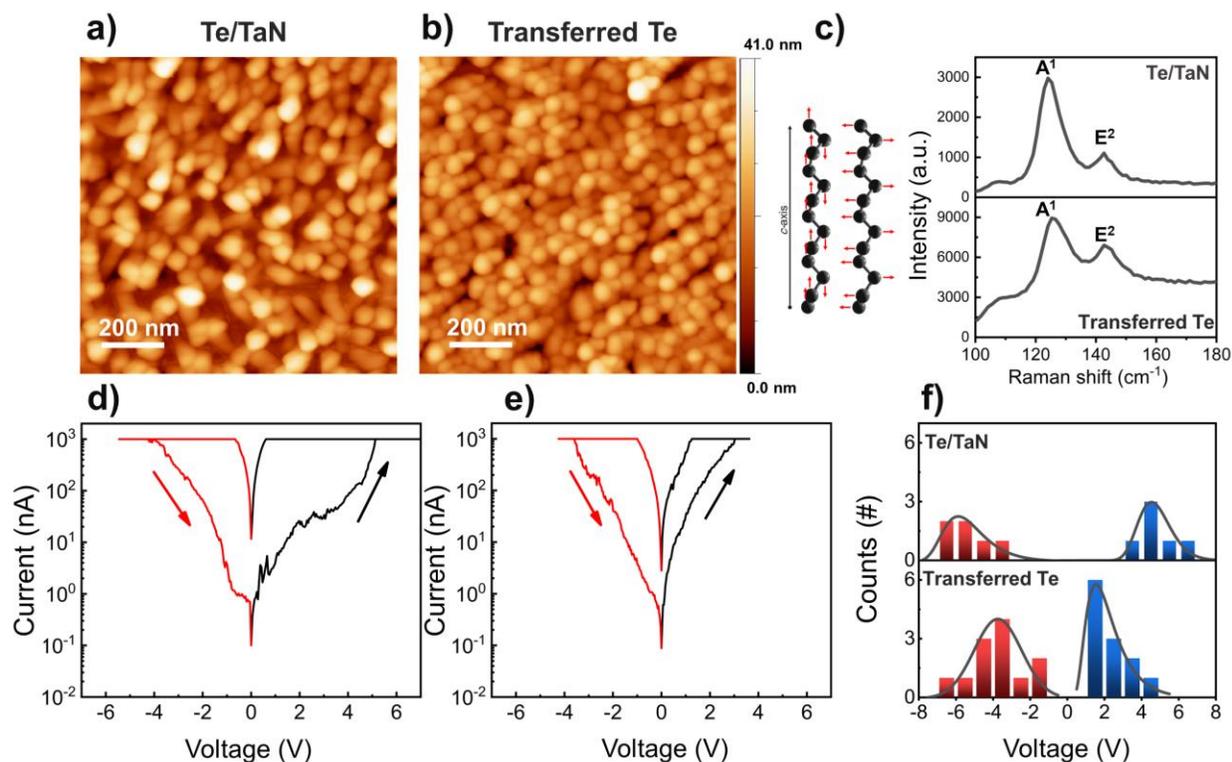
such as chemical sensors<sup>38,39</sup> and field effect transistors<sup>33,40-42</sup>. However, to date, the examination of the RS effect of synthetic tellurene at the nanoscale and at the device level is relatively unexplored.

As part of the investigation into the relatively new field of tellurium-based RS devices, the influence of the substrate is revealed to be a significant factor in defining the overall operation of the device. The choice of substrate is pivotal in shaping how tellurium reconfigures within a memristor-suited layout. Thus, the development of a synthesis method is crucial to achieve large-scale ultra-thin films of tellurium that may be applied to a variety of conductive substrates serving as bottom electrodes (BE).

In this work, we discuss the RS effect observed in ultra-scaled tellurium films deposited on a large scale by the vapor transport deposition (VTD) method at a sufficient low temperature suitable for the effective exploitation of conductive materials as supporting substrates. Specifically, we use tantalum nitride (TaN) and gold (Au) as substrates ensuring compatibility with the back-end-of-line (BEOL) circuit fabrication process flow. To validate the RS behavior of tellurium at the local scale, we utilize the conductive atomic force microscopy (C-AFM) technique, where the nanoprobe acts as a localized top electrode. Furthermore, we extend our investigation to the device level focusing on Au-based substrates patterning by optical lithography of the top electrodes. This study lays the groundwork for the utilization of ultra-thin tellurium directly deposited on metallic substrates for the investigation of memristive devices in flexible and technology-compliant platforms readily transferable to edge-computing systems.

## RESULTS and DISCUSSION

The experimental results of the VTD of ultra-thin tellurium on TaN and SiO<sub>2</sub>/Si substrates are summarized in **Figure 1**. Although the TaN substrate is suitable as the bottom electrode (BE) to test the RS behavior of the tellurium films deposited on top, conversely, for the SiO<sub>2</sub>/Si case, it is necessary to detach the deposited material and transfer it to a conductive supporting substrate. As a result, in the following, we discuss the characteristics of the transferred tellurium on the Au (111) substrate, which has been also used for direct growth (see below). More details on the transfer methodology can be found in the Experimental Section and Supporting Information.



**Figure 1.** AFM topography image performed on 1  $\mu\text{m} \times 1 \mu\text{m}$  scan area of tellurium thin-films a) directly grown on TaN substrate and b) transferred on Au substrate. c) Raman spectroscopy acquired on tellurium thin-films grown on TaN substrate (top) and tellurium thin-films transferred

on Au substrate (bottom). I-V characteristics obtained by C-AFM performed on tellurium thin-films d) directly grown on TaN substrate e) transferred on Au substrate f) Distribution of set (blue) and reset (red) voltages for tellurium thin-films grown on TaN substrate (top) and tellurium thin-films transferred on Au substrate (bottom).

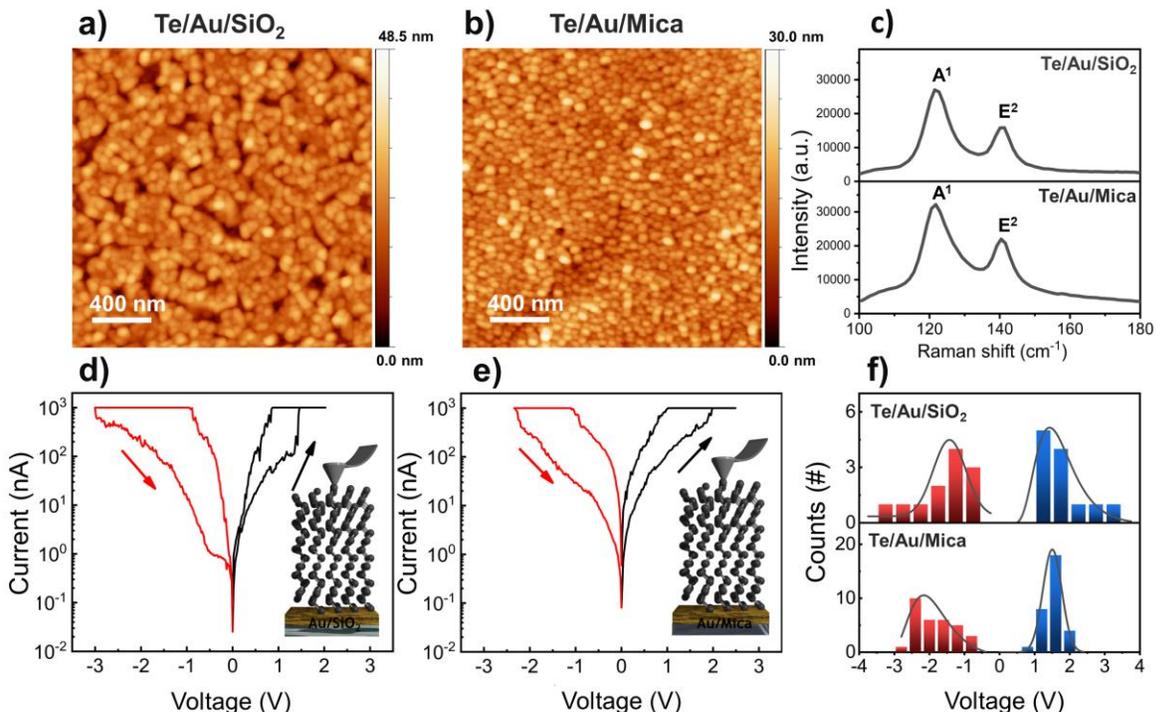
The high-resolution AFM morphology images measured on  $1\ \mu\text{m} \times 1\ \mu\text{m}$  scan area of tellurium grown on TaN and transferred tellurium are represented in **Figure 1 a-b**, respectively. Based on the cross-correlation method, the topographies show the formation of tellurium grains with typical grain sizes of 55 and 50 nm for tellurium grown on TaN and transferred tellurium on Au respectively (more details in the supporting information see **Figure SI-1**).

The Raman spectra of both the samples (**Figure 1 c**) present two main peaks at 124.5 and 142.6  $\text{cm}^{-1}$  for tellurium grown on TaN, and 125.8 and 143.4  $\text{cm}^{-1}$  for transferred tellurium. These peaks are assigned to the  $A^1$  and  $E^2$  Raman active modes of the tellurium lattice in agreement with previous studies<sup>30,35,43</sup>. These two modes correspond to the out-of-plane, characteristics of basal plane stretching along the  $a$ -direction and in-plane active mode due to asymmetric axial-chain stretching along the  $c$ -direction of the tellurium lattice (see inset of Figure 1c)<sup>35</sup>. We stress that, along with the AFM characterization, Raman spectroscopy is routinely used to assess the quality of transferred films as well as 2D materials<sup>44</sup>. Therefore, the evidence that the width and the relative intensity of the characteristic Raman peaks are comparable in the as-grown and transferred material leads us to the conclusion that the polymer-assisted transfer methodology has a negligible impact on the quality of the tellurium film placed onto the Au (111) supporting substrate.

We used C-AFM to locally investigate the vertical electrical transport properties of the samples by recording the current between the conductive tip and the substrate in contact mode, thus acquiring

the topographic and current maps simultaneously. A more interesting picture of the electrical properties of the tellurium film is derived by the acquisition of point spectroscopy current-voltage ( $I$ - $V$ ) curves on a statistical set of points in the AFM maps. **Figure 1 d-e** show some representative  $I$ - $V$  curves at specific points of the as-grown and transferred tellurium where a clear hysteretic feature can be observed by sweeping back the  $I$ - $V$  scanning which is indicative of an RS behavior. In detail, tellurium film on TaN featured low currents corresponding to a high resistive state (HRS) until the application of  $\sim 5.1$  V (set voltage). At the set voltage, the material switched to a low resistive state (LRS) that persists until a negative voltage around  $-4.2$  V is applied thus resetting the LRS back to HRS. Interestingly, a similar RS behavior is observed in the transferred film when a gold substrate is used as BE, with the difference that the set and reset voltages are reduced to the values of  $3.0$  and  $-3.5$  V respectively. We further notice that the hysteresis behavior observed in both the  $I$ - $V$  curves in **Figure 1** is ambipolar in character since the HRS-to-LRS and the LRS-to-HRS switches occur at the opposite bias polarity. The set and reset voltage distributions corresponding to all the hysteresis  $I$ - $V$  measures are plotted in **Figure 1f**. In the case of tellurium grown on TaN, the set voltage values span from  $4.2$  to  $6.2$  V, and simultaneously the reset voltages fall within the range of  $-7$  to  $-6$  V. For the transferred tellurium, the set voltage values vary between  $1.4$  to  $4.2$  V thus reflecting a decrease compared to the TaN substrate. Conversely, the reset voltages span from  $-6.5$  to  $-1.2$  V thereby pointing out a shift toward more negative values. The observed voltage changes indicate how the RS behavior changes under various substrate conditions. More importantly, the behavior of the  $I$ - $V$  curves directly proves that the deposited tellurium films behave as a switch in selected points only thereby suggesting an intrinsic origin of the mechanism in monoelemental tellurium film being present in both the samples. This observation echoes what has already been observed in switching devices based on  $20$  nm thick Te

cells, where the switching mechanism consists of a transition from crystalline to liquid phases of the Te films induced by the Joule heating effect.<sup>45</sup>



**Figure 2.** AFM topography image performed on  $2\ \mu\text{m} \times 2\ \mu\text{m}$  scan area of tellurium thin-films directly grown on a) Au/SiO<sub>2</sub> substrate and b) Au/Mica substrate. c) Raman spectroscopy acquired on tellurium thin-films directly grown on Au/SiO<sub>2</sub> substrate (top) and on Au/Mica substrate (bottom). I-V characteristics obtained by C-AFM performed on tellurium thin-films directly grown on d) Au/SiO<sub>2</sub> substrate e) Au/Mica substrate f) Distribution of set and reset voltages for tellurium thin-films grown on Au/SiO<sub>2</sub> substrate (top) Au/Mica substrate (bottom).

Motivated by the observation of the RS in the deposited tellurium films and having demonstrated that the growth can be obtained at temperature as low as 100 °C<sup>28</sup>, the growths are carried out directly on gold substrates, the same used for the transferred tellurium, for the relevance that this metal has in many RS systems<sup>46</sup> and to rule out any effect of polymer contamination during the

transfer procedure. Moreover, the direct growth on gold represents a technological step towards the “transfer-free” and “litho-free” approaches for the creation of devices with clean interfaces between the active material and the electrode, taking advantage of the intrinsic inert nature of gold against oxidation.<sup>47</sup> Furthermore, not only Au provides a functional platform for memristive cell fabrication, but we also demonstrate that it plays a crucial role in boosting memristive performance. We anticipate that keeping the growth conditions under control is crucial for preventing the formation of AuTe<sub>2</sub> as a result of the reaction between Au and Te. In particular, we found out that the temperature of the gold substrate should not exceed 350 °C.<sup>48</sup>

**Figures 2 a-b** show typical AFM images of as-deposited tellurium on evaporated Au (~50 nm) and thin (~300 nm-thick) Au (111) on mica substrate, respectively on a 2 μm × 2 μm scan area. While the former substrate turns out to be polycrystalline, the latter one is a single crystal thin film. The two morphologies bring evidence of continuous films consisting of small grains with average grain sizes of 65 and 48 nm for tellurium grown on Au/SiO<sub>2</sub> and Au (111)/Mica respectively.

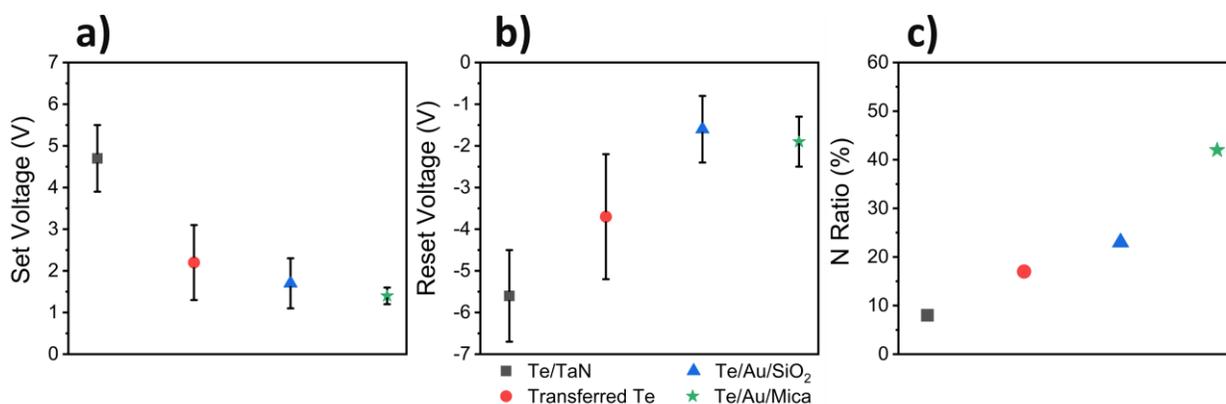
A direct comparison of the spectra reported in **Figure 2 c** reveals that the Raman modes of the tellurium grown on evaporated Au substrate match with those detected on the equivalent deposition carried out on the crystalline substrate. This is confirmed by the two peaks at 121.7 and 140.8 cm<sup>-1</sup> associated with A<sup>1</sup> out-of-plane and E<sup>2</sup> in-plane vibrational modes of Te, which turn out to be slightly redshifted with respect to those of tellurium grown on TaN (**Figure 1 c**).

As for the previous cases, the local C-AFM point-spectroscopies in **Figure 2 d-e** enable us to investigate the vertical transport properties of the samples more specifically. **Figures 2 d-e** show the representative *I-V* curves acquired on tellurium grown on Au/SiO<sub>2</sub> and Au(111)/Mica respectively. For the tellurium grown on Au/SiO<sub>2</sub>, as the positive voltage sweeps from 0 to 2 V, the set voltage is at 1.4 V where the transition from HRS to LRS occurs. During the negative bias,

the resistance is switched back to HRS at the reset voltage of  $-3$  V. For the tellurium grown on Au (111)/Mica the set voltage is  $1.9$  V and as the voltage decreases toward negative values at the average reset voltage of  $-2.3$  V there is a switch back to HRS. The switching performance observed in tellurium directly grown on different gold substrates exhibits a bipolar RS behavior. The double-logarithmic  $I$ - $V$  curves for the set and reset processes of ultra-thin tellurium films grown on Au/Mica (Figure 2e) are depicted in **Figure SI-2**. The histogram distribution of set and reset voltages for all the hysteresis  $I$ - $V$  curves acquired from tellurium grown on Au/SiO<sub>2</sub> and Au(111)/Mica is reported in **Figure 2 f**. The set voltage for tellurium grown on Au/SiO<sub>2</sub> spans from  $1.1$  to  $3.2$  V and the reset voltage falls within the  $-3.3$  up to  $-0.6$  V. For the tellurium grown on Au(111)/Mica the set voltage value is between  $0.8$  to  $2$  V and the reset voltage value is between  $-2.7$  to  $-1$  V.

In **Figure 3 a-b**, the C-AFM measurements were analyzed to compare the average values and variations of both set and reset voltages of the tellurium films grown directly on gold substrates with those deposited on TaN substrates and the films initially deposited on SiO<sub>2</sub>/Si substrates and later transferred on gold substrates. Since surface Au atoms are expected to be highly mobile under growth, it is interesting to assess if the Au substrate in the direct growth scheme plays an extra-role in triggering the RS effect compared to the other cases in point. Notably, the average set voltage values and their variations for tellurium directly grown on Au/SiO<sub>2</sub> and Au(111)/Mica substrates are calculated to be  $1.7 \pm 0.6$  V and  $1.4 \pm 0.2$  V respectively which are lower than those of transferred tellurium  $2.2 \pm 0.9$  V and of the tellurium grown on TaN substrate  $4.7 \pm 0.8$  V. Furthermore, the average values of the reset voltage and their variations for the tellurium directly grown on Au/SiO<sub>2</sub> and Au(111)/Mica substrates are calculated to be  $-1.6 \pm 0.8$  V and  $-1.9 \pm 0.6$  V

while the corresponding values for the transferred tellurium and tellurium grown on TaN are  $-3.7 \pm 1.5$  V and  $-5.6 \pm 1.1$  V. On the other hand, **Figure 3 c** summarizes the ratio (N) of the number of points with hysteresis RS behavior to the total number of acquired  $I$ - $V$  curves. The overall comparison elucidates that the samples directly grown on Au substrates considerably increase the number of RS points, whereas the transferred tellurium sample and tellurium grown on TaN exhibit much lower percentages of RS points in the probed area (18% and 7% respectively).



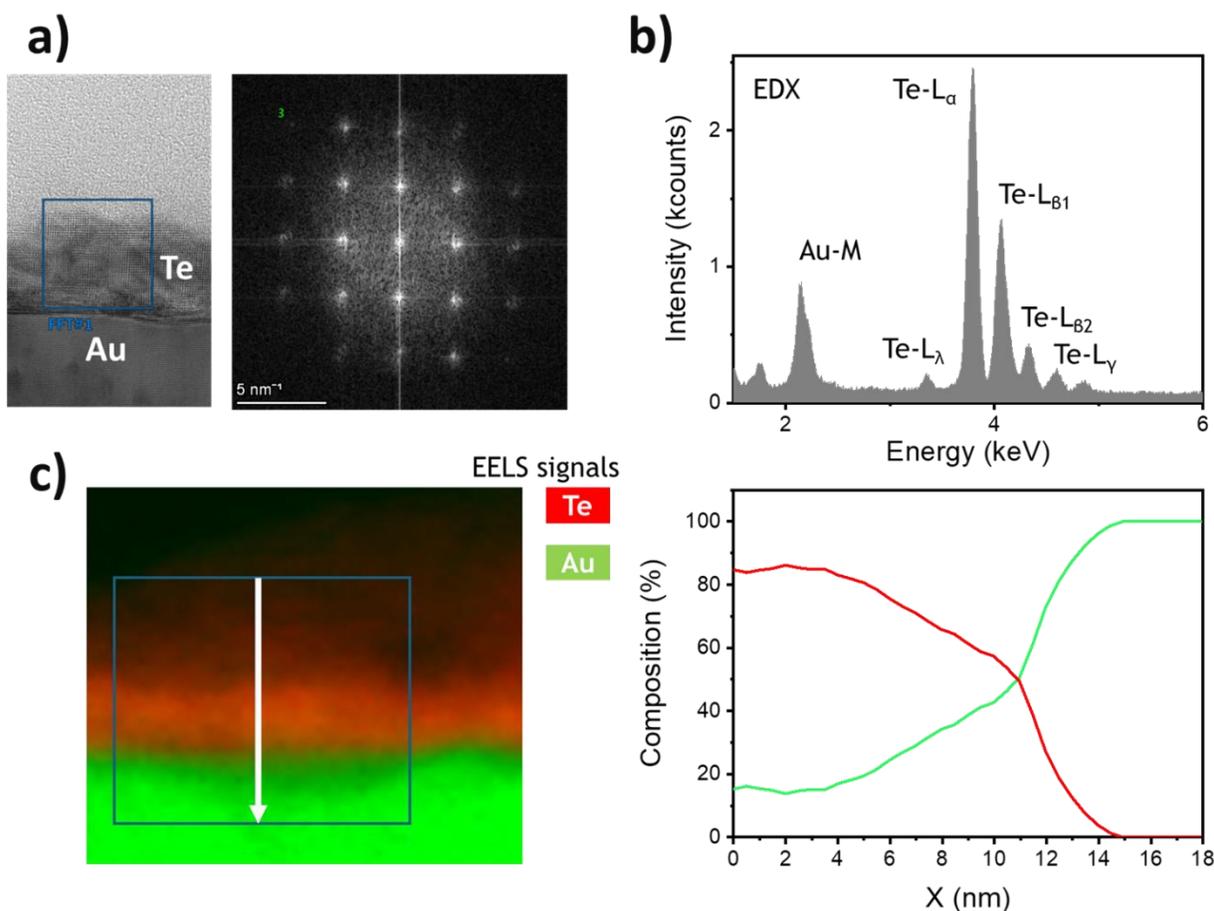
**Figure 3.** a) The average value and standard deviations of set voltages of different ultra-thin tellurium films b) the average value and standard deviations of different ultra-thin tellurium films c) the calculated N ratio, representing the ratio of number of points with hysteresis RS behavior to the total number of acquired  $I$ - $V$  curves in different ultra-thin tellurium films.

The lower average set and reset voltages and their variations and the higher yield of directly grown tellurium on Au substrates suggest the favorable characteristics of the direct growth method in terms of the reduction of voltage and energy consumption. Such a comparison better clarifies that the best RS performances, in terms of reduction of the set voltages and (hence of power consumption), are observed in the samples obtained by the direct deposition of tellurium on Au. This fact points to a primary role of the Au substrate in boosting the intrinsic RS behavior of the

tellurium film. As a matter of fact, Au has been used as conductive material for the BE in memristor devices based on MoS<sub>2</sub> (atomristor) as an active layer.<sup>23</sup> In such an atomristor configuration, the RS behavior has been attributed to the gold ion migration from the BE through the atomic vacancies located into the MoS<sub>2</sub> active layer<sup>49</sup>. We notice that the local nature of the C-AFM measurements is typically called out to attribute the origin of the RS behavior to a filamentary conduction mechanism.

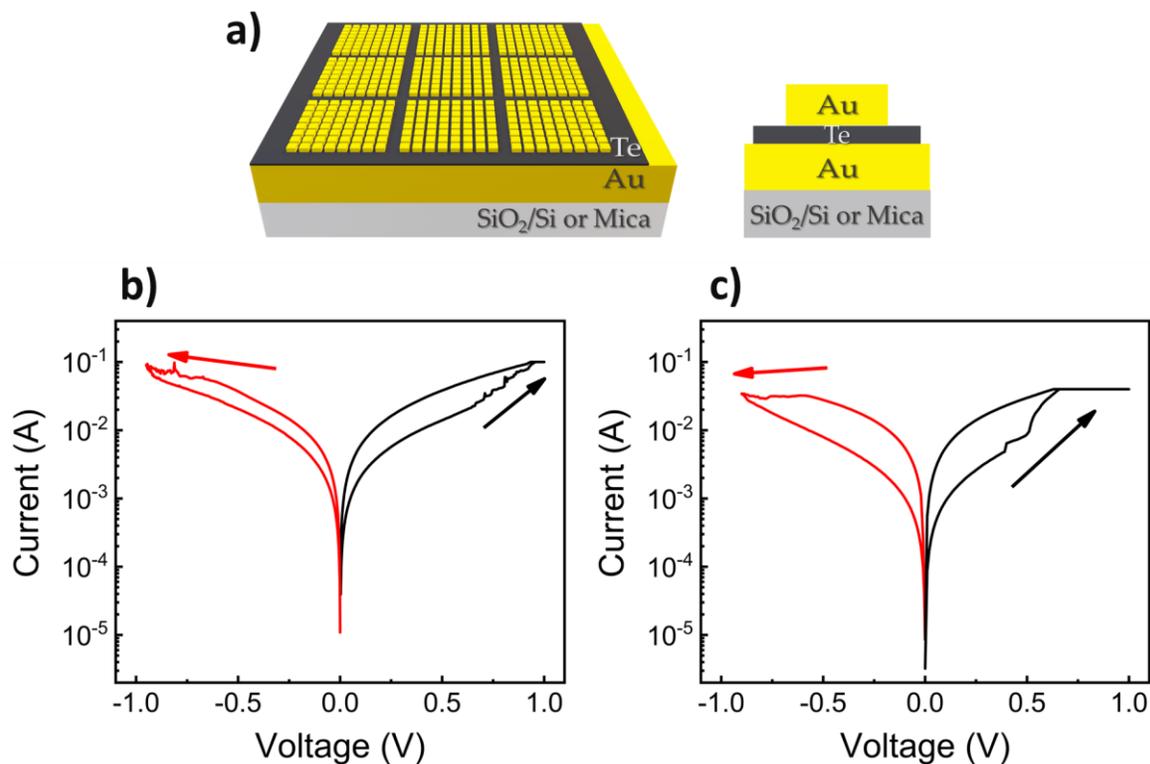
To have a closer insight into this aspect and thus unveil the origin of the RS mechanism, cross-sectional images of the tellurium film deposited on gold substrates were acquired using an aberration-corrected scanning transmission electron microscopy (STEM). The deposited tellurium film is fully crystalline as assessed by calculating the electron diffraction pattern of the lattice by fast Fourier transform (FFT) corresponding to the rectangular box in **Figure 4 a**. While the Te layer appears homogeneous in the STEM micrograph (**Figure 4 a left**), the corresponding energy-dispersive x-ray spectroscopy (EDX) (**Figure 4 b**) reveals that both the elements are present in the deposited material. We emphasize that, while the most prominent peaks in the EDX spectrum correspond to the L-subshell of Te, a significant presence of Au is identified by the M-subshell of gold peaked at ~2.2 keV. This fact demonstrates that even the low thermal budget of the Te deposition at 100 °C is sufficient to activate the diffusion mechanism of the gold atoms from the substrate into the deposited material. Since the EDX analysis typically suffers from poor spatial resolution, we display in **Figure 4 c** also the electron energy-loss spectroscopy (EELS) graphs acquired in the rectangular selection of the STEM image. The EELS offers very high spatial resolution and enables us a detailed elemental analysis of the deposited material<sup>50</sup>. Notably, we find that Te and Au signals overlap over a scale of several nanometers at the interface of the two materials, which is clearly displayed in the spectrum extracted along the path indicated in the

energy-loss map, **Figure 4 c**. In this overlapping region, the percent composition of the elements can be semi-quantitatively assessed by using the Hartree-Slater scattering cross-sections of the M shells of the elements implemented in the analysis software, it results the following concentrations: Te  $60\% \pm 9\%$  and Au  $40\% \pm 6\%$ .<sup>50</sup>



**Figure 4.** a) cross-sectional STEM images showing the deposited Te film on the Au substrate along with the FFT electron diffraction pattern of the lattice corresponding to the region of the blue box. b) EDXS spectrum showing the detected electronic shells of Au and Te atoms in the same box of a) .c) EELS map and percent composition along the path in figure (white arrow). The spatial distribution of Au and Te shows that the two energy-loss signals overlap at the interface over a scale of several nanometers.

Motivated by the local memristive character of the tellurium nanosheets and taking benefit from the low-temperature process, the RS behavior is explored in a memristor planar single-cell structures where the conductive substrates, either polycrystalline Au/SiO<sub>2</sub> or crystalline Au (111)/Mica, act as bottom electrodes. Each memristive cell consists of an RS active media made by an ultra-thin film of tellurium (15 nm thickness) via direct VTD growth at the same growth condition as the previous section, a bottom electrode made from the Au-based substrate, and a top electrode made by polycrystalline Au subsequently deposited by e-beam evaporation (see sketch in **Figure 5 a** and for details see **Figure SI-3**). The ultra-thin film of tellurium constituting the RS media is directly grown on a substrate, while polycrystalline Au is deposited on top through e-beam evaporation to function as the top electrode for both types of bottom electrodes. The top electrodes are patterned by an optical lithography technique designed with a set of square layouts each comprising 8 × 8 squares with 15 × 15 μm<sup>2</sup> electrode area. After the fabrication, the electrical characterization of devices is performed at the DC probe station. **Figure 5 b-c** represent the *I-V* characteristics of the ultra-thin film of tellurium memristor based on Au/SiO<sub>2</sub> and Au/Mica substrates. The memristors show the non-volatile bipolar RS behavior with set voltage values of 0.78 and 0.66 V for memristors based on Au/SiO<sub>2</sub> and Au/Mica bottom electrodes, respectively. Reset voltage values for memristors based on Au/SiO<sub>2</sub> and Au/Mica bottom electrodes are – 0.64 and – 0.89 V respectively. It is worth noticing that the set and absolute value of reset voltages of the developed tellurium memristor devices are falling below 1 V, thus making them suitable for low-power electronics applications. **Figure SI-4** represents a further analysis using the double-logarithmic *I-V* plot for the set and reset processes of **Figure 5 c**, the memristor device based on Au/Mica.



**Figure 5.** a) schematic representation of the vertical Au/tellurium/Au memristor device, showing Au/SiO<sub>2</sub> or Au/Mica substrates serve as bottom electrodes, deposited ultra-thin tellurium films on substrates and square patterned top electrodes b) I-V characteristics of the ultra-thin tellurium film memristor device based on Au/SiO<sub>2</sub> bottom electrode c) I-V characteristics of the ultra-thin tellurium film memristor based on Au/Mica bottom electrode.

The exploitation of the Au/Mica as a platform for memristor devices opens the door to the realization of flexible memristors using delamination in the form of membrane as reported for the case of silicene.<sup>51,52</sup> Notably, our findings demonstrate that the local scale RS mechanism demonstrated by the C-AFM characterization is suitable for the implementation and realization of real memristor devices.

## CONCLUSION

We investigate the potential of large-area ultra-scaled tellurium films grown via the VTD method at low temperatures to exhibit a non-volatile bipolar RS behavior. Memristors based on nanoscale tellurium nanosheets exhibit a non-volatile bipolar resistive switching behavior both at the local scale in C-AFM probing and in micro-scale cells. Memristors of this kind were produced on several configurations including the direct growth on TaN and Au-based substrates, or the growth-and-transfer to a secondary substrate. In particular, we show that memristor devices fabricated via direct growth on Au-based substrate achieve a remarkably low record of set voltage. This reflects the pivotal contribution of the gold substrate as a bottom electrode in the performance enhancement of tellurium-based memristors. This finding opens a wide room to investigate parametric optimization of the so-developed tellurium-based memristors and to engineer them in flexible circuitry taking benefit from the extraction of nanoscale tellurium membrane enabled by the reported synthesis method. Furthermore, the exploitation of tellurium film heterostructures with other 2D materials can be explored to develop innovative memristor designs with enhanced characteristics.

## **METHODS**

**Materials growth: Vapor Transport Deposition.** two different gold substrates were used for the experiments: i) 50 nm -thick gold film was deposited onto SiO<sub>2</sub> (50 nm)/Si substrate employing

e-beam evaporation. ii) commercial Au (111) single crystal with nominal thickness  $\sim 300$  nm on mica substrate. The deposition reactor consists of a double furnace system equipped with a quartz tube reactor of 2'' diameter. Tellurium (Te) powder (40 mg: 99.997%, Sigma Aldrich, Darmstadt, Germany) was used as a precursor. The tellurium powder was placed in a ceramic boat in the center of the upstream furnace, and the gold substrate was cut in  $3\text{ cm} \times 1\text{ cm}$  dimensions, kept on a ceramic boat (face up), and positioned 18 cm away from the Te precursor reference. The temperatures of 450 °C set for the upstream and 100 °C set for the downstream, with a 100 sccm Ar/H<sub>2</sub> flux (H<sub>2</sub> 4% volume) as a carrier gas that was flowing for 30 minutes growth time.

### **Transfer methods**

The transfer process of centimeter-scale tellurium was done by HF transfer. First, a layer of Poly(methyl methacrylate) (PMMA) was spin-coated with 1500 rpm spinning speed onto the Te/SiO<sub>2</sub>/Si stack acting as a support layer and then baked at 80 °C for 15 minutes. Then, the PMMA/Te stack was floated in HF solution until complete detachment from underneath the SiO<sub>2</sub>/Si substrate. Once the PMMA/Te stack was detached, the floating stack was fished to the target Au substrate and baked at 90 °C for 1 minute. The remaining PMMA was removed by acetone completing the transfer process.

### **Sample characterization.**

**Atomic Force Microscopy (AFM):** The morphology of the samples was investigated in tapping mode using commercial AFM (Bruker Dimension Edge). Topographies were acquired in tapping mode using ultra-sharp silicon tips (TESPA-V2 Bruker radius of curvature 7 nm nominal frequency 320 kHz) Statistical parameters of the surface morphology, such as root-mean-square (RMS) Roughness, were derived by means of freely available software (WSxM, Gwyddion).

### **Conductive AFM (C-AFM):**

The commercial AFM (Bruker Dimension Edge) equipped with a TUNA electrometer with 1 pA to 1  $\mu$ A current range was used to characterize the electrical properties of the samples at the local scale. A conductive diamond-coated tip (CDT-CONTR, nanosensors, with a radius of curvature between 100 nm and 200 nm) was used to scan over the surface of the sample.

**Raman spectroscopy:** The vibrational properties of the deposited sample were verified by Raman spectroscopy in z-backscattering geometry using a Renishaw spectrometer (In-Via) equipped with a solid-state laser source of excitation wavelength 514 nm / 2.41 eV. The laser source is coupled with an optical microscope () and objective with numerical aperture = 0.75 and magnification 50 $\times$ . The laser power on the sample was kept below 5 mW to avoid sample damage.

**Electrical testing:** The planar single-cell structure Te memristor was measured to verify electrical characteristics using the Keithley 4200-SCS semiconductor parameter ultrafast module and a 4225-RPM pulse signal unit. All measurements were carried out by controlling the top electrode bias and fixing the bottom electrode as ground.

### **Transmission electron microscopy (TEM) and EDX o EELS**

The samples were extensively investigated utilizing scanning transmission electron microscopy (STEM) related techniques such as dark-field STEM (DF-STEM) for the microstructural characterization, while the chemical properties were investigated by STEM-EELS and STEM EDX. DF-STEM, EDX, and EELS analyses were carried out on electron-transparent lamella obtained using focused ion beam (FIB) thinning of cross-section TEM lamellae. The lamellae preparation was performed using a Thermofischer Helios G5UX FIB. In all the cases, particular

care was taken to limit the heating and ballistic effects of ion irradiation on the samples during the final ion milling steps. In particular, a new advanced approach has been applied, reducing currents and energies progressively from a value of 30 keV to a value of low keV in order to avoid material amorphization and damage. The STEM images were performed with a Thermofischer Themis Z G3 aberration-corrected scanning transmission electron microscope equipped with an electron gun monochromator operating at 200 kV acceleration voltage. To limit the electron beam damage, all the STEM images, EDX, and EELS maps were acquired with a low beam current (0.5 nA). The EELS experiments were performed with the post-column Quantum Gatan imaging filter operating with an energy resolution of 1 eV/channel. The GST elemental maps were obtained with a step size of 8 Å, and the data were processed using the Gatan® GMS Digital Micrograph 3.23 software.

### **Sample processing**

The electrical contacts were made by defining three vertical series of 8×8 squares, each with a distance of 200 μm and varying lateral dimensions of 15 μm. The patterning was carried out using Tabletop Maskless Aligner μMLA (from Heidelberg) and a special photoresist (AZ5241), well-designed for lift-off techniques. After depositing 50 nm-thick of Au via e-beam deposition (Auto 304 from Edward) over a patterned photoresist, lift-off was performed using acetone.

### ASSOCIATED CONTENT

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## AUTHOR CONTRIBUTIONS

All authors have given approval to the final version of the manuscript. ‡These authors contributed equally. (match statement to author names with a symbol)

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## NOTES

The authors declare no competing financial interest.

## ACKNOWLEDGMENT

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## References

- (1) von Neumann, J. First Draft of a Report on the EDVAC. *IEEE Annals of the History of Computing* **1993**, *15* (4), 27–75. <https://doi.org/10.1109/85.238389>.
- (2) Christensen, D. V.; Dittmann, R.; Linares-Barranco, B.; Sebastian, A.; Gallo, M. L.; Redaelli, A.; Slesazek, S.; Mikolajick, T.; Spiga, S.; Menzel, S.; Valov, I.; Milano, G.; Ricciardi, C.; Liang, S.-J.; Miao, F.; Lanza, M.; Quill, T. J.; Keene, S. T.; Salleo, A.; Grollier, J.; Marković, D.; Mizrahi, A.; Yao, P.; Yang, J. J.; Indiveri, G.; Strachan, J. P.; Datta, S.; Vianello, E.; Valentian, A.; Feldmann, J.; Li, X.; Pernice, W. H. P.; Bhaskaran, H.; Furber, S.; Neftci, E.; Scherr, F.; Maass, W.; Ramaswamy, S.; Tapson, J.; Panda, P.; Kim, Y.; Tanaka, G.; Thorpe, S.; Bartolozzi, C.; Cleland, T. A.; Posch, C.; Liu, S.; Panuccio, G.; Mahmud, M.; Mazumder, A. N.; Hosseini, M.; Mohsenin, T.; Donati, E.; Tolu, S.; Galeazzi, R.; Christensen, M. E.; Holm, S.; Ielmini, D.; Pryds,

N. 2022 Roadmap on Neuromorphic Computing and Engineering. *Neuromorph. Comput. Eng.* **2022**, 2 (2), 022501. <https://doi.org/10.1088/2634-4386/ac4a83>.

(3) Lanza, M.; Sebastian, A.; Lu, W. D.; Le Gallo, M.; Chang, M.-F.; Akinwande, D.; Puglisi, F. M.; Alshareef, H. N.; Liu, M.; Roldan, J. B. Memristive Technologies for Data Storage, Computation, Encryption, and Radio-Frequency Communication. *Science* **2022**, 376 (6597), eabj9979. <https://doi.org/10.1126/science.abj9979>.

(4) Lee, J. S.; Lee, S.; Noh, T. W. Resistive Switching Phenomena: A Review of Statistical Physics Approaches. *Applied Physics Reviews* **2015**, 2 (3), 031303. <https://doi.org/10.1063/1.4929512>.

(5) Chua, L. Memristor-The Missing Circuit Element. *IEEE Transactions on Circuit Theory* **1971**, 18 (5), 507–519. <https://doi.org/10.1109/TCT.1971.1083337>.

(6) Williams, R. S. How We Found The Missing Memristor. *IEEE Spectrum* **2008**, 45 (12), 28–35. <https://doi.org/10.1109/MSPEC.2008.4687366>.

(7) Ielmini, D. Resistive Switching Memories Based on Metal Oxides: Mechanisms, Reliability and Scaling. *Semicond. Sci. Technol.* **2016**, 31 (6), 063002. <https://doi.org/10.1088/0268-1242/31/6/063002>.

(8) Nakamura, H.; Rungger, I.; Sanvito, S.; Inoue, N.; Tominaga, J.; Asai, Y. Resistive Switching Mechanism of GeTe–Sb<sub>2</sub>Te<sub>3</sub> Interfacial Phase Change Memory and Topological Properties of Embedded Two-Dimensional States. *Nanoscale* **2017**, 9 (27), 9386–9395. <https://doi.org/10.1039/C7NR03495D>.

(9) Zou, X.; Ong, H. G.; You, L.; Chen, W.; Ding, H.; Funakubo, H.; Chen, L.; Wang, J. Charge Trapping-Detrapping Induced Resistive Switching in Ba<sub>0.7</sub>Sr<sub>0.3</sub>TiO<sub>3</sub>. *AIP Advances* **2012**, 2 (3), 032166. <https://doi.org/10.1063/1.4754150>.

(10) Xue, F.; He, X.; Ma, Y.; Zheng, D.; Zhang, C.; Li, L.-J.; He, J.-H.; Yu, B.; Zhang, X. Unraveling the Origin of Ferroelectric Resistance Switching through the Interfacial Engineering of Layered Ferroelectric-Metal Junctions. *Nat Commun* **2021**, 12 (1), 7291. <https://doi.org/10.1038/s41467-021-27617-6>.

(11) Kent, A. D.; Worledge, D. C. A New Spin on Magnetic Memories. *Nature Nanotech* **2015**, 10 (3), 187–191. <https://doi.org/10.1038/nnano.2015.24>.

(12) Bhat, T. S.; Revadekar, C. C.; Patil, S. S.; Dongale, T. D.; Kim, D.; Patil, P. S. Photo-Induced Resistive Switching in CdS-Sensitized TiO<sub>2</sub> Nanorod Array Memristive Device. *J Mater Sci: Mater Electron* **2020**, 31 (13), 10919–10929. <https://doi.org/10.1007/s10854-020-03643-w>.

(13) Memory with a Spin. *Nature Nanotech* **2015**, 10 (3), 185–185. <https://doi.org/10.1038/nnano.2015.50>.

(14) Zahoor, F.; Azni Zulkifli, T. Z.; Khanday, F. A. Resistive Random Access Memory (RRAM): An Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (MLC) Storage, Modeling, and Applications. *Nanoscale Res Lett* **2020**, 15 (1), 90. <https://doi.org/10.1186/s11671-020-03299-9>.

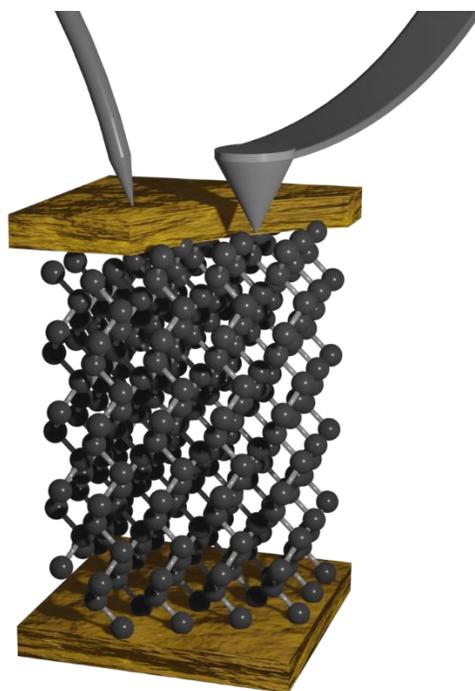
- (15) Waser, R.; Aono, M. Nanoionics-Based Resistive Switching Memories. *Nature Mater* **2007**, *6* (11), 833–840. <https://doi.org/10.1038/nmat2023>.
- (16) Sun, K.; Chen, J.; Yan, X. The Future of Memristors: Materials Engineering and Neural Networks. *Advanced Functional Materials* **2021**, *31* (8), 2006773. <https://doi.org/10.1002/adfm.202006773>.
- (17) Sawa, A. Resistive Switching in Transition Metal Oxides. *Materials Today* **2008**, *11* (6), 28–36. [https://doi.org/10.1016/S1369-7021\(08\)70119-6](https://doi.org/10.1016/S1369-7021(08)70119-6).
- (18) Huh, W.; Lee, D.; Lee, C.-H. Memristors Based on 2D Materials as an Artificial Synapse for Neuromorphic Electronics. *Advanced Materials* **2020**, *32* (51), 2002092. <https://doi.org/10.1002/adma.202002092>.
- (19) Hui, F.; Grustan-Gutierrez, E.; Long, S.; Liu, Q.; Ott, A. K.; Ferrari, A. C.; Lanza, M. Graphene and Related Materials for Resistive Random Access Memories. *Advanced Electronic Materials* **2017**, *3* (8), 1600195. <https://doi.org/10.1002/aelm.201600195>.
- (20) Wu, X.; Ge, R.; Chen, P.-A.; Chou, H.; Zhang, Z.; Zhang, Y.; Banerjee, S.; Chiang, M.-H.; Lee, J. C.; Akinwande, D. Thinnest Nonvolatile Memory Based on Monolayer H-BN. *Advanced Materials* **2019**, *31* (15), 1806790. <https://doi.org/10.1002/adma.201806790>.
- (21) Shen, Y.; Zheng, W.; Zhu, K.; Xiao, Y.; Wen, C.; Liu, Y.; Jing, X.; Lanza, M. Variability and Yield in H-BN-Based Memristive Circuits: The Role of Each Type of Defect. *Advanced Materials* **2021**, *33* (41), 2103656. <https://doi.org/10.1002/adma.202103656>.
- (22) Xie, J.; Afshari, S.; Sanchez Esqueda, I. Hexagonal Boron Nitride (h-BN) Memristor Arrays for Analog-Based Machine Learning Hardware. *npj 2D Mater Appl* **2022**, *6* (1), 1–7. <https://doi.org/10.1038/s41699-022-00328-2>.
- (23) Ge, R.; Wu, X.; Kim, M.; Shi, J.; Sonde, S.; Tao, L.; Zhang, Y.; Lee, J. C.; Akinwande, D. Atomristor: Nonvolatile Resistance Switching in Atomic Sheets of Transition Metal Dichalcogenides. *Nano Lett.* **2018**, *18* (1), 434–441. <https://doi.org/10.1021/acs.nanolett.7b04342>.
- (24) Ge, R.; Wu, X.; Liang, L.; Hus, S. M.; Gu, Y.; Okogbue, E.; Chou, H.; Shi, J.; Zhang, Y.; Banerjee, S. K.; Jung, Y.; Lee, J. C.; Akinwande, D. A Library of Atomically Thin 2D Materials Featuring the Conductive-Point Resistive Switching Phenomenon. *Advanced Materials* **2021**, *33* (7), 2007792. <https://doi.org/10.1002/adma.202007792>.
- (25) Yan, X.; Zheng, Z.; Sangwan, V. K.; Qian, J. H.; Wang, X.; Liu, S. E.; Watanabe, K.; Taniguchi, T.; Xu, S.-Y.; Jarillo-Herrero, P.; Ma, Q.; Hersam, M. C. Moiré Synaptic Transistor with Room-Temperature Neuromorphic Functionality. *Nature* **2023**, *624* (7992), 551–556. <https://doi.org/10.1038/s41586-023-06791-1>.
- (27) Kumar, D.; Li, H.; Das, U. K.; Syed, A. M.; El-Atab, N. Flexible Solution-Processable Black-Phosphorus-Based Optoelectronic Memristive Synapses for Neuromorphic Computing and Artificial Visual Perception Applications. *Advanced Materials* **2023**, *35* (28), 2300446. <https://doi.org/10.1002/adma.202300446>.

- (28) Ghomi, S.; Tummala, P. P.; Cecchini, R.; Casari, C. S.; Lamperti, A.; Grazianetti, C.; Martella, C.; Molle, A. Tailoring the Dimensionality of Tellurium Nanostructures via Vapor Transport Growth. *Materials Science in Semiconductor Processing* **2023**, *168*, 107838. <https://doi.org/10.1016/j.mssp.2023.107838>.
- (29) Grazianetti, C.; Martella, C. The Rise of the Xenos: From the Synthesis to the Integration Processes for Electronics and Photonics. *Materials* **2021**, *14* (15), 4170. <https://doi.org/10.3390/ma14154170>.
- (30) Du, Y.; Qiu, G.; Wang, Y.; Si, M.; Xu, X.; Wu, W.; Ye, P. D. One-Dimensional van Der Waals Material Tellurium: Raman Spectroscopy under Strain and Magneto-Transport. *Nano Lett.* **2017**, *17* (6), 3965–3973. <https://doi.org/10.1021/acs.nanolett.7b01717>.
- (31) Zhu, Z.; Cai, X.; Yi, S.; Chen, J.; Dai, Y.; Niu, C.; Guo, Z.; Xie, M.; Liu, F.; Cho, J.-H.; Jia, Y.; Zhang, Z. Multivalency-Driven Formation of Te-Based Monolayer Materials: A Combined First-Principles and Experimental Study. *Phys. Rev. Lett.* **2017**, *119* (10), 106101. <https://doi.org/10.1103/PhysRevLett.119.106101>.
- (32) Huang, X.; Guan, J.; Lin, Z.; Liu, B.; Xing, S.; Wang, W.; Guo, J. Epitaxial Growth and Band Structure of Te Film on Graphene. *Nano Lett.* **2017**, *17* (8), 4619–4623. <https://doi.org/10.1021/acs.nanolett.7b01029>.
- (33) Wang, Y.; Qiu, G.; Wang, R.; Huang, S.; Wang, Q.; Liu, Y.; Du, Y.; Goddard, W. A.; Kim, M. J.; Xu, X.; Ye, P. D.; Wu, W. Field-Effect Transistors Made from Solution-Grown Two-Dimensional Tellurene. *Nat Electron* **2018**, *1* (4), 228–236. <https://doi.org/10.1038/s41928-018-0058-4>.
- (34) Hussain, N.; Rafique, M.; Anwar, T.; Murtaza, M.; Liu, J.; Nosheen, F.; Huang, K.; Huang, Y.; Lang, J.; Wu, H. A High-Pressure Mechanism for Realizing Sub-10 Nm Tellurium Nanoflakes on Arbitrary Substrates. *2D Mater.* **2019**, *6* (4), 045006. <https://doi.org/10.1088/2053-1583/ab2540>.
- (35) Bianco, E.; Rao, R.; Snure, M.; Back, T.; Glavin, N. R.; McConney, M. E.; Ajayan, P. M.; Ringe, E. Large-Area Ultrathin Te Films with Substrate-Tunable Orientation. *Nanoscale* **2020**, *12* (23), 12613–12622. <https://doi.org/10.1039/D0NR01251C>.
- (36) Sang, D. K.; Wen, B.; Gao, S.; Zeng, Y.; Meng, F.; Guo, Z.; Zhang, H. Electronic and Optical Properties of Two-Dimensional Tellurene: From First-Principles Calculations. *Nanomaterials* **2019**, *9* (8), 1075. <https://doi.org/10.3390/nano9081075>.
- (37) Shi, Z.; Cao, R.; Khan, K.; Tareen, A. K.; Liu, X.; Liang, W.; Zhang, Y.; Ma, C.; Guo, Z.; Luo, X.; Zhang, H. Two-Dimensional Tellurium: Progress, Challenges, and Prospects. *Nanomicro Lett* **2020**, *12*, 99. <https://doi.org/10.1007/s40820-020-00427-z>.
- (38) Wang, D.; Yang, A.; Lan, T.; Fan, C.; Pan, J.; Liu, Z.; Chu, J.; Yuan, H.; Wang, X.; Rong, M.; Koratkar, N. Tellurene Based Chemical Sensor. *J. Mater. Chem. A* **2019**, *7* (46), 26326–26333. <https://doi.org/10.1039/C9TA09429F>.

- (39) Cui, H.; Zheng, K.; Xie, Z.; Yu, J.; Zhu, X.; Ren, H.; Wang, Z.; Zhang, F.; Li, X.; Tao, L.-Q.; Zhang, H.; Chen, X. Tellurene Nanoflake-Based NO<sub>2</sub> Sensors with Superior Sensitivity and a Sub-Parts-per-Billion Detection Limit. *ACS Appl. Mater. Interfaces* **2020**, *12* (42), 47704–47713. <https://doi.org/10.1021/acsami.0c15964>.
- (40) Zhao, C.; Tan, C.; Lien, D.-H.; Song, X.; Amani, M.; Hettick, M.; Nyein, H. Y. Y.; Yuan, Z.; Li, L.; Scott, M. C.; Javey, A. Evaporated Tellurium Thin Films for P-Type Field-Effect Transistors and Circuits. *Nat. Nanotechnol.* **2020**, *15* (1), 53–58. <https://doi.org/10.1038/s41565-019-0585-9>.
- (41) Kim, T.; Choi, C. H.; Byeon, P.; Lee, M.; Song, A.; Chung, K.-B.; Han, S.; Chung, S.-Y.; Park, K.-S.; Jeong, J. K. Growth of High-Quality Semiconducting Tellurium Films for High-Performance p-Channel Field-Effect Transistors with Wafer-Scale Uniformity. *npj 2D Mater Appl* **2022**, *6* (1), 1–7. <https://doi.org/10.1038/s41699-021-00280-7>.
- (42) Chen, A.; Ye, S.; Wang, Z.; Han, Y.; Cai, J.; Li, J. Machine-Learning-Assisted Rational Design of 2D Doped Tellurene for Fin Field-Effect Transistor Devices. *Patterns* **2023**, *4* (4), 100722. <https://doi.org/10.1016/j.patter.2023.100722>.
- (43) Zhao, X.; Shi, J.; Yin, Q.; Dong, Z.; Zhang, Y.; Kang, L.; Yu, Q.; Chen, C.; Li, J.; Liu, X.; Zhang, K. Controllable Synthesis of High-Quality Two-Dimensional Tellurium by a Facile Chemical Vapor Transport Strategy. *iScience* **2022**, *25* (1), 103594. <https://doi.org/10.1016/j.isci.2021.103594>.
- (44) Ferrari, A. C.; Basko, D. M. Raman Spectroscopy as a Versatile Tool for Studying the Properties of Graphene. *Nature Nanotech* **2013**, *8* (4), 235–246. <https://doi.org/10.1038/nnano.2013.46>.
- (45) Shen, J.; Jia, S.; Shi, N.; Ge, Q.; Gotoh, T.; Lv, S.; Liu, Q.; Dronskowski, R.; Elliott, S. R.; Song, Z.; Zhu, M. Elemental Electrical Switch Enabling Phase Segregation-Free Operation. *Science* **2021**, *374* (6573), 1390–1394. <https://doi.org/10.1126/science.abi6332>.
- (46) Zhang, Z.; Ji, X.; Shi, J.; Zhou, X.; Zhang, S.; Hou, Y.; Qi, Y.; Fang, Q.; Ji, Q.; Zhang, Y.; Hong, M.; Yang, P.; Liu, X.; Zhang, Q.; Liao, L.; Jin, C.; Liu, Z.; Zhang, Y. Direct Chemical Vapor Deposition Growth and Band-Gap Characterization of MoS<sub>2</sub>/h-BN van Der Waals Heterostructures on Au Foils. *ACS Nano* **2017**, *11* (4), 4328–4336. <https://doi.org/10.1021/acsnano.7b01537>.
- (47) Ge, R.; Wu, X.; Kim, M.; Lee, J. C.; Akinwande, D. 1 - Two-Dimensional Materials-Based Nonvolatile Resistive Memories and Radio Frequency Switches. In *Emerging 2D Materials and Devices for the Internet of Things*; Tao, L., Akinwande, D., Eds.; Micro and Nano Technologies; Elsevier, 2020; pp 1–28. <https://doi.org/10.1016/B978-0-12-818386-1.00001-1>.
- (48) Ghomi, S.; Lamperti, A.; Alia, M.; Casari, C. S.; Grazianetti, C.; Molle, A.; Martella, C. Large Area Growth of Silver and Gold Telluride Ultrathin Films via Chemical Vapor Tellurization. *Inorganics* **2024**, *12* (1), 33. <https://doi.org/10.3390/inorganics12010033>.

- (49) Hus, S. M.; Ge, R.; Chen, P.-A.; Liang, L.; Donnelly, G. E.; Ko, W.; Huang, F.; Chiang, M.-H.; Li, A.-P.; Akinwande, D. Observation of Single-Defect Memristor in an MoS<sub>2</sub> Atomic Sheet. *Nat. Nanotechnol.* **2021**, *16* (1), 58–62. <https://doi.org/10.1038/s41565-020-00789-w>.
- (50) Egerton, R. F. Electron Energy-Loss Spectroscopy in the TEM. *Rep. Prog. Phys.* **2008**, *72* (1), 016502. <https://doi.org/10.1088/0034-4885/72/1/016502>.
- (51) Martella, C.; Faraone, G.; Alam, M. H.; Taneja, D.; Tao, L.; Scavia, G.; Bonera, E.; Grazianetti, C.; Akinwande, D.; Molle, A. Disassembling Silicene from Native Substrate and Transferring onto an Arbitrary Target Substrate. *Advanced Functional Materials* **2020**, *30* (42), 2004546. <https://doi.org/10.1002/adfm.202004546>.
- (52) Martella, C.; Massetti, C.; Dhungana, D. S.; Bonera, E.; Grazianetti, C.; Molle, A. Bendable Silicene Membranes. *Advanced Materials* **2023**, *35* (49), 2211419. <https://doi.org/10.1002/adma.202211419>.
- (53) Lin, W.; Zhuang, P.; Akinwande, D.; Zhang, X.-A.; Cai, W. Oxygen-Assisted Synthesis of hBN Films for Resistive Random Access Memories. *Applied Physics Letters* **2019**, *115* (7), 073101. <https://doi.org/10.1063/1.5100495>.

TOC



## Supporting Information

# Non-volatile resistive switching in nanoscaled elemental tellurium by vapor transport deposition on gold

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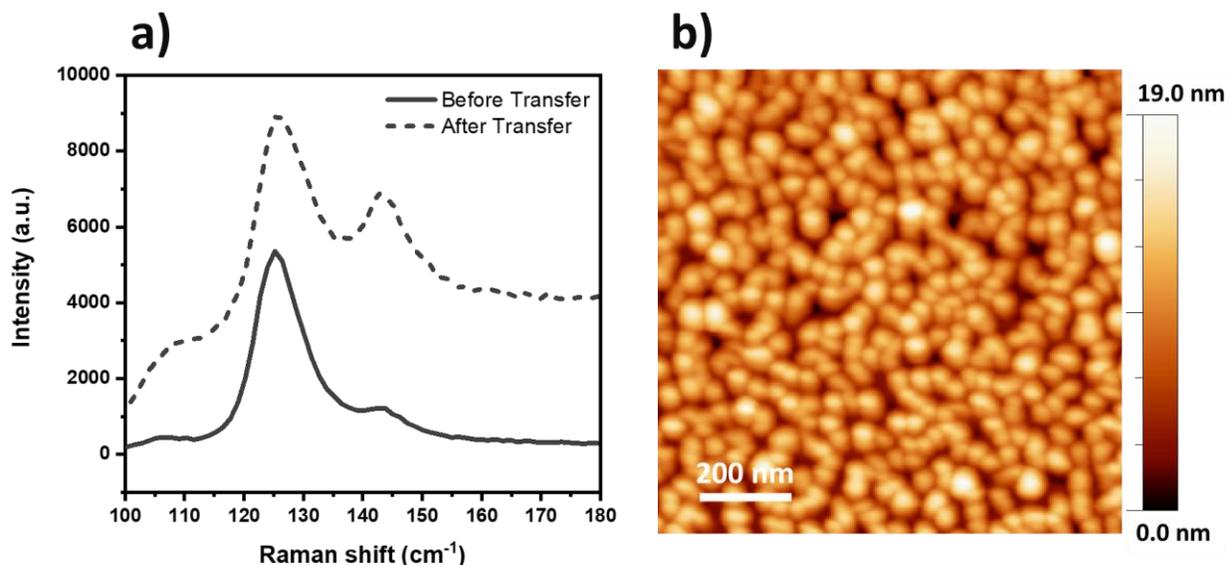
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*1) Raman spectroscopy and AFM performed on ultra-thin tellurium film grown on SiO<sub>2</sub>/Si substrate before transfer on Au/Mica substrate*

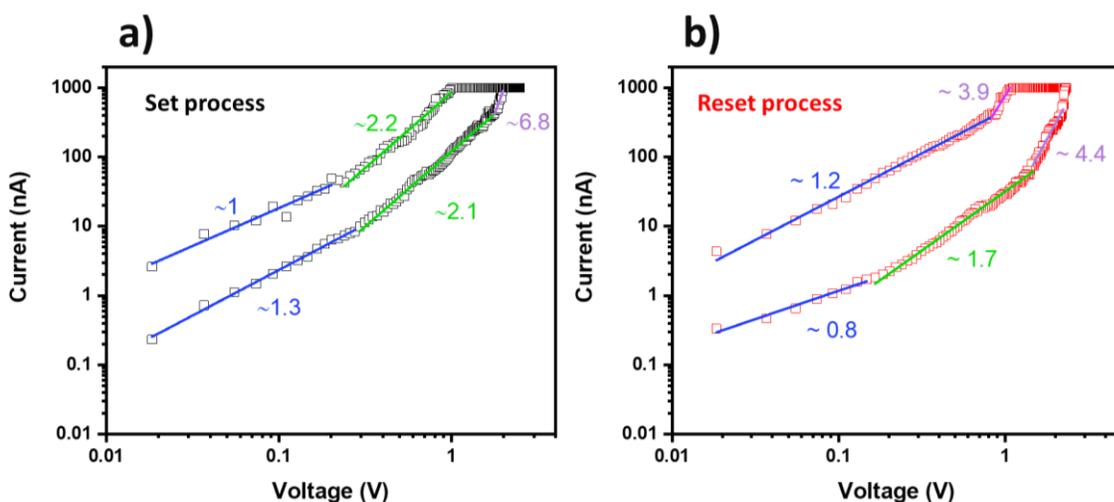
The Raman spectra were acquired on the tellurium sample grown on SiO<sub>2</sub>/Si, before transfer (solid line), and after transfer on Au (111)/Mica (dashed line) process. The peak positions remain approximately unchanged, while the intensity of the peaks arises after the transfer due to the background coming from the gold substrate.



**Figure SI-1** a) Raman spectra acquired on the ultra-thin tellurium film grown on SiO<sub>2</sub>/Si substrate before (solid line) and after (dashed line) transfer to the Au substrate b) AFM topography image performed on 1  $\mu\text{m} \times 1 \mu\text{m}$  scan area of the ultra-thin tellurium film grown on SiO<sub>2</sub>/Si substrate before transfer.

## 2) Revealing the conduction mechanism at the local scale through $\log(|I|)$ vs. $\log(|V|)$ plot

To further investigate the RS mechanism, the  $I$ - $V$  characteristics of the tellurium films on Au(111)/Mica substrates during set and reset processes are plotted in a double-logarithmic axis (see **Figures SI-2**). Analyzing the slope of the linear fit at various segments of the double-logarithmic plot provides insights into the underlying conduction mechanism. During the set process, the  $I$ - $V$  curve in the LRS displays the slope of  $\approx 1$  indicating the current and voltage are following Ohm's law ( $I \approx V$ ) which suggests the conductive filament formation.<sup>53</sup> In the HRS, the initial slope shows the linear correlation associated with the ohmic conduction mechanism. As the voltage gradually increases, the slope shows a quadratic relation indicating transition to a space charge limit conduction mechanism (SCLC). Subsequently, the slope undergoes an abrupt jump reaching 6.8, indicative of a shift from trap-unfilled to trap-filled SCLC mechanism. The different conductive characteristics in HRS and LRS highlight the charge transport in the LRS is characterized by localized behavior, aligning with the conductive filament formation mechanism<sup>53</sup>. A similar process is occurring at negative voltages during the reset process.

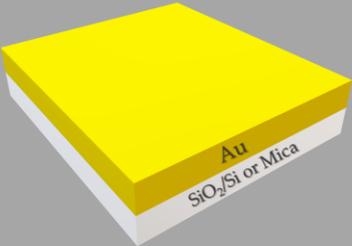
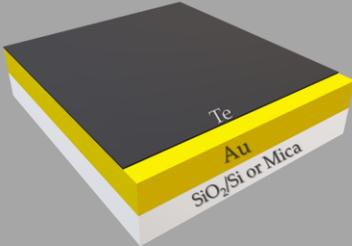
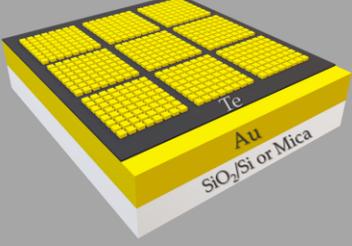


**Figure SI-2** Double-logarithmic plots of the  $I$ - $V$  characteristics shown in Figure 2 e of ultra-thin tellurium films grown on Au (111)/Mica in a) positive bias region (set process) and b) negative bias region (reset process).

### 3) Illustration model of resistive switching behavior at the local scale

According to the literature, the driving forces behind the formation of conductive filaments and resistive switching behavior in thin films include the complex interplay between various factors. One contributor is the presence of vacancies introduced naturally in the films. Simultaneously, the diffusion of gold atoms within the film matrix, potentially facilitated due to the existence of vacancies, adds another dimension to the mechanism. A voltage sweep can trigger the gold atoms within the film due to its tendency to be absorbed into the vacancies, facilitated by the negative adsorption energy observed for the adsorption of gold into a vacancy site in various 2D materials.<sup>24</sup> Increasing the voltage can lead to the accumulation of gold atoms and complete the formation of conductive paths, leading to the SET process. Then, sweeping the negative voltage initiates the removal of gold atoms from defects causing the RESET process and restoring the resistance state.

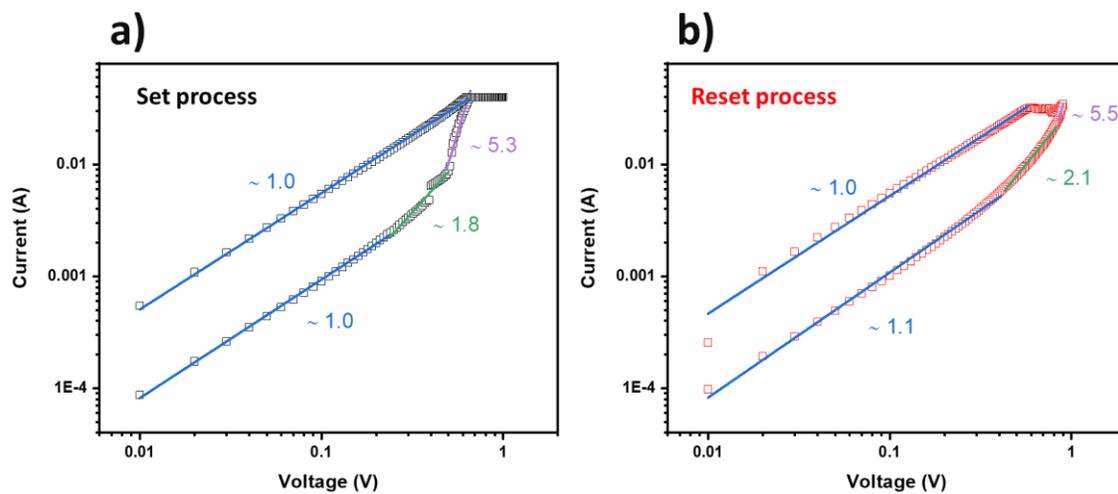
### 4) Memristor device fabrication process based on tellurium film deposited on Au substrates

<b>a) Bottom electrode:</b> Au deposited on SiO <sub>2</sub> /Si or Mica	<b>b) Resistive switching material:</b> Direct VTD growth of ultra-thin tellurium films on Au bottom electrode	<b>c) Top electrode:</b> Pattern lithography, deposition of Au top electrode by thermal evaporation and lift-off
		

**Figure SI-3** schematic illustration of memristor device fabrication process a) Au deposited on SiO<sub>2</sub>/Si or Mica substrates acting as bottom electrode b) direct vapor transport deposition growth of ultra-thin tellurium films on Au bottom electrode c) top electrode definition after the pattern lithography, deposition of 50 nm-thick Au top electrode by thermal evaporation and lift-off process.

### ***5) Revealing the conduction mechanism at the device level through $\log(|I|)$ vs. $\log(|V|)$ plot***

To investigate the RS behavior of ultra-thin tellurium films at the memristor device level, the  $I$ - $V$  characteristics of the Au/Te/Au/Mica during SET and RESET processes are plotted in a double-logarithmic axis. During the SET process, the HRS can be divided into three regions which are linearly fitted with different slopes. At the initial region, the slope is  $\approx 1$  indicative of the ohmic conduction mechanism due to the existence of thermally generated carriers or trapped charges. As the applied voltage increases, the slope undergoes a transition to  $\approx 1.8$  signifying trap unfilled SCLC mechanism, due to the presence of traps, e.g., vacancies inside material. Increasing the voltage will lead to a sharp increase in the slope to the value of  $\approx 5.3$ , transforming to trap-filled SCLC thus, leading to the SET process. Then, at the LRS, the slope is  $\approx 1$  indicating the ohmic conduction behavior and confirming the complete formation of a conductive filament path between the top and bottom electrodes.



**Figure SI-4** Double-logarithmic plots of the  $I$ - $V$  characteristics obtained at the device level of ultra-thin tellurium films grown on Au (111)/Mica (shown in Figure 5c) in a) positive bias region (set process) and b) negative bias region (reset process).