Sub-3V, MHz-Class Electrolyte-Gated Transistors and Inverters

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Abstract

Electrolyte-gated transistors (EGTs) have emerging applications in physiological recording, neuromorphic computing, sensing, and flexible printed electronics. A challenge for these devices is their slow switching speed, which has several causes. Here we report the fabrication and characterization of n-type ZnO-based EGTs with signal propagation delays as short as 70 ns. Propagation delays are assessed in dynamically operating inverters and five stage ring oscillators as a function of channel dimensions and supply voltages up to 3V. Substantial decreases in switching time are realized by minimizing parasitic resistances and capacitances that are associated with the electrolyte in these devices. Stable switching at 1-10 MHz is achieved in individual inverter stages with 10-40 μm channel lengths, and analysis suggests that further improvements are possible.

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Introduction

The use of polarized electrolytes to modulate or "gate" the conductance of a semiconducting channel is an old idea that has its origins in the development of the first solid-state transistors at Bell Labs in the 1940s [1]. There are now many examples of semiconductor devices that can generally be called electrolyte-gated transistors (EGTs)[2,3], though they go by different names. Over the last 70 years, EGTs have had several rebirths associated with the development of new EGT applications, or new materials that enhance performance, or discovery of new transport phenomena within EGTs. The ion-sensitive field effect transistor (ISFET) developed in the 1970s is an early example of an EGT[4,5], where ion adsorption on gate oxides of Si FETs is exploited to make high sensitivity ion sensors. Microelectrochemical transistors, extensively developed by Wrighton and coworkers in the 1980s[6,7], were another important milestone. These devices employ gate potentials to modulate the conductivity of conducting polymers in direct contact with electrolyte. Currently, EGTs are again enjoying a resurgence of interest associated with their applications in physiological recording[8–10], neuromorphic computing[11–16], and biosensing[17–22], as well as in fundamental physics[23–26], where the high charge densities achieved in electrolyte-gated semiconductors are leading to exciting discoveries.

A principal problem with EGTs for many applications is that their switching speed is limited[2]. This is easily understandable because the mechanisms of electrolyte gating rely on ion fluxes to form electrical double layers at the gate/electrolyte and semiconductor/electrolyte interfaces, or – in the electrochemical mode – to penetrate into the semiconductor. Ion mobilities are orders of magnitude smaller than electron or hole mobilities in semiconductors, which means the ionic resistance of the intervening electrolyte between the gate electrode and the semiconductor channel is relatively large. This ionic resistance can be viewed as a parasitic resistance R_p in series

with the gate and it is dependent on intrinsic electrolyte conductivity, electrolyte thickness, and cross-sectional area[27–29]. As we demonstrate below, for an EGT-based circuit it can unfortunately be the case that the limiting ON-state resistance R_{total}^{ON} controlling signal propagation delay is not determined by the semiconductor channel resistance $R_{channel}^{ON}$, or the source/drain contact resistance $R_{contact}^{ON}$, but rather is dominated by R_p due to slow ion motion in the electrolyte (i.e., $R_{total}^{ON} = R_{channel}^{ON} + R_{contact}^{ON} + R_p$, where R_p dominates[30–32]). We, and others, have measured ionic conductivity for gel electrolyte films based on ionic liquids and polymers and found it to be as large as 4 mS/cm depending on the precise gel composition[33–35]. Thus, for typical EGTs with channel areas of ~1000 μm^2, and gel film thicknesses of ~1 μm, R_p is on the order of 1 kΩ, which is a large value. Less resistive, ultrathin gate electrolyte films are a clear goal for EGTs[36]. Khodagholy and coworkers[8] have recently minimized electrolyte polarization times by mixing gel electrolytes with a semiconducting polymer to make a composite mixed ionic and electronic channel material. In their EGTs, single current step rise and fall times of 1 μs were achieved, which they argued were due to short migration path lengths for ions between electronically conducting polymer domains and internal, phase-separated ion reservoirs. However, R_p was not reported in that work and continuous MHz-level switching was not demonstrated.

Another challenge for EGT switching speed is parasitic capacitance, C_p[30–32]. Parasitic capacitance arises from contact between the electrolyte and the source and drain electrodes of the transistor. Specifically, the double layer polarization of the source/electrolyte and drain/electrolyte interfaces must change when the gate voltage switches. Thus, the double-layer capacitances of these interfaces, lumped together, constitute C_p, which is in parallel with the electrolyte-channel capacitance, $C_{channel}$. The presence of parasitic capacitance increases the total ON-state capacitive load C_{total}^{ON} that the gate must switch, i.e., $C_{total}^{ON} = C_{channel}^{ON} + C_p$. This in turn increases the EGT

signal propagation delay τ in a circuit. If one takes the common approximation that $\tau \approx R_{total}^{ON} C_{total}^{ON}$ (reasonable for inverters described below), then it becomes clear that for optimized operation (smallest τ) not only must R_p be minimized so that $R_p << (R_{channel}^{ON} + R_{contact}^{ON})$, but $C_p << C_{channel}^{ON}$.

The role of parasitic capacitance is well-recognized in thin film transistor (TFT) technology where it is also a problem[37]. C_p is minimized in conventional TFTs by reducing the projected areal overlap between the gate and the source and drain electrodes. For EGTs, the parasitic penalty on τ is exacerbated by the enormous specific capacitance associated with metal/electrolyte interfaces, of order 10 μF/cm^2, which means that essentially any source/electrolyte or drain/electrolyte contact results in relatively large C_p.

In this work, we apply these ideas to fabricate fast EGTs and EGT circuits, and we establish that MHz-class devices can be realized with switching delays below 100 ns for the fastest devices. In our view there are clear reasons why EGTs will not rival the speed of Si MOSFETs[2] (though perhaps not everyone agrees[38]), but for envisioned applications of EGTs, gigahertz speeds do not appear necessary. As EGTs are being developed as physiological recording amplifiers[9,10], and integrated into circuits[36,39–41] and neural nets[4,11,13,14,16], it is nevertheless important to establish the limits of performance that can be obtained by rational design. We note that there are other limitations to EGT performance like high dielectric loss tangents and quasi-static leak currents associated with electrolytes that are important for power consumption[2], but these are not our focus here.

Results and Discussion

Our EGT device design is shown in Figure 1a. We employ a thin film of ZnO as the semiconductor channel because of its high electron mobility (~5 cm^2/Vs), its stability in contact

with electrolytes, and its ease of growth and patterning by atomic layer deposition (ALD) and photolithography[32,42]. The source and drain electrodes are Au/Ti and channel lengths *L* are systematically varied from 10 - 40 μm, scaling the channel width *W* such that the aspect ratio is fixed at *W/L* = 20, unless otherwise noted. The electrolyte is a soft solid called an ion gel that we

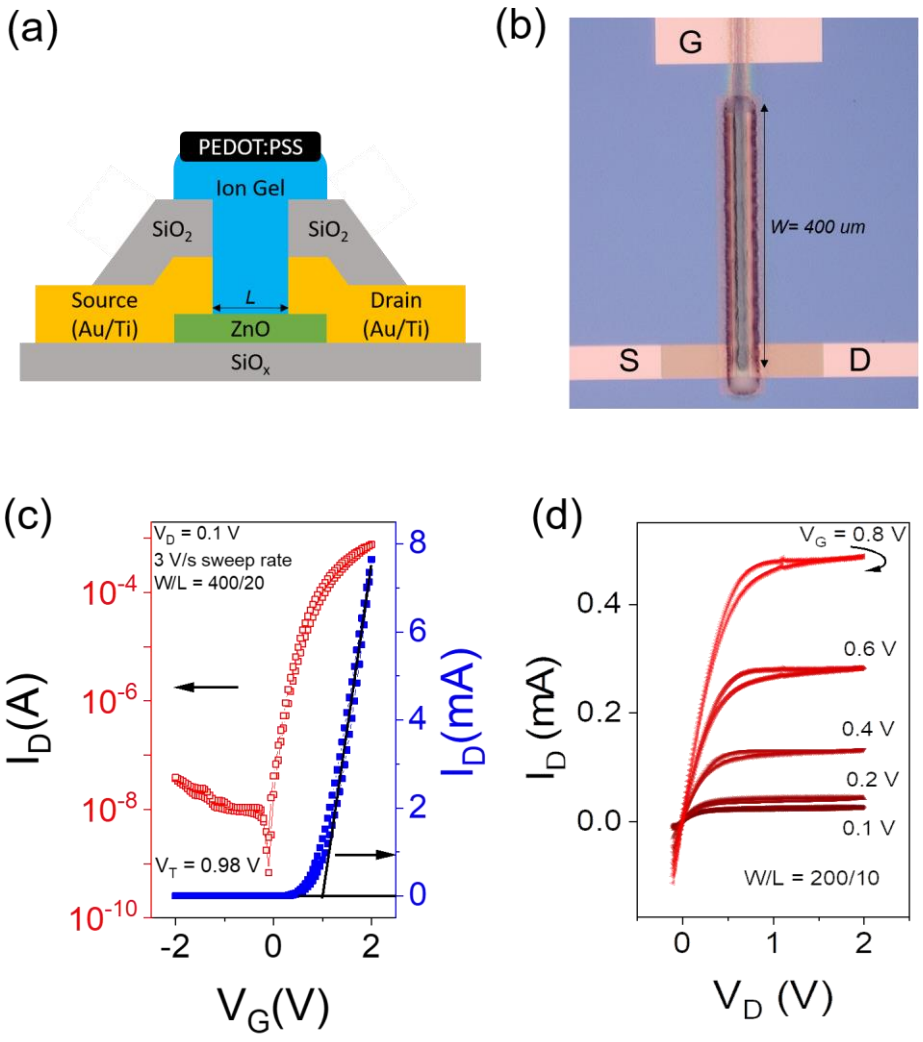

Figure 1. (A) Scheme of an n-channel ZnO EGT. The SiO_2 insulating overlayers on top of the source and drain electrodes reduce parasitic capacitance C_p by minimizing electrolyte/metal contact. Channel length *L* is indicated. (B) Plan view photograph of a completed EGT. Channel width *W*=400 μm as shown. (C) Quasi-static I_D-V_G (transfer) characteristic on log and linear scales for an n-channel ZnO EGT with *W/L* = 400 μm/20 μm. V_D = 0.1 V and V_G sweep rate is 3 V/s. (D) Corresponding quasistatic I_D-V_D (output) characteristics as a function of V_G. V_D sweep rate is 3 V/s.

and others have developed previously for EGTs[43–45]. Its attributes are high ionic conductivity (~4 mS/cm), a wide electrochemical stability window, chemical inertness, hydrophobicity, which allows it to serve as a kind of channel encapsulation, and its facile patterning by aerosol jetting. The gate electrode is also aerosol jet printed and is make of the conducting polymer PEDOT:PSS, which has a large volumetric capacitance (~1 F/cm^3) by virtue of its permeability to ions. The large volumetric capacitance reduces the impedance of the PEDOT/ion gel interface and ensures that when a gate voltage V_G is applied, that the majority of the voltage drops at the electrical double layer formed at the smaller, impermeable ion gel/ZnO interface. Importantly, the broad top surfaces of the Au source and drain electrodes are insulated from the ion gel by patterned SiO_x overlayers in order to reduce the parasitic capacitance. Figure 1b shows an optical micrograph of a completed ZnO EGT; images of the devices at various stages of completion are shown in Supporting Information (see Figure S1).

Typical quasi-static drain current (I_D) - gate voltage (V_G) curves are displayed in Figure 1c for an EGT with W/L = 400 μm/20 μm. One sees minor hysteresis in the forward and reverse sweeps at a gate voltage sweep rate of 3 V/s. The threshold voltage V_T = +1 V, the sub-threshold current onset occurs at V_G = 0 V, and the ON/OFF ratio is 10^5. The relatively large OFF current of 10 nA (see Figure S2 in Supporting Information) can be attributed to the large size of the device and the inherent leakage through electrolytes, which is often due to impurities such as H_2O (the PEDOT gate is printed from an aqueous ink). The corresponding output curves (I_D vs drain voltage V_D) are shown in Figure 1d. The device exhibits reasonable saturation and square law current scaling up to V_G = +0.8 V. Beyond V_G = +0.8 V, I_D increases, but not quadratically (see Supporting Information, Figure S3). This behavior reflects the mobility saturation that occurs at larger gate voltages.

To characterize parasitic resistances and capacitances that affect dynamic performance, we have undertaken impedance analysis of the ZnO EGTs as a function of voltage and frequency. Figure 2a shows an equivalent circuit for an EGT in which gate-source and gate-drain parasitic capacitances C_p are identified, as well as the parasitic resistance R_p, due to a combination of the ionic resistance of the electrolyte between the gate and the channel, discussed above, and the resistance of the PEDOT gate. In the two terminal impedance measurement, the source and drain are grounded and a small AC bias (50 mV amplitude) with a DC offset is applied to the PEDOT

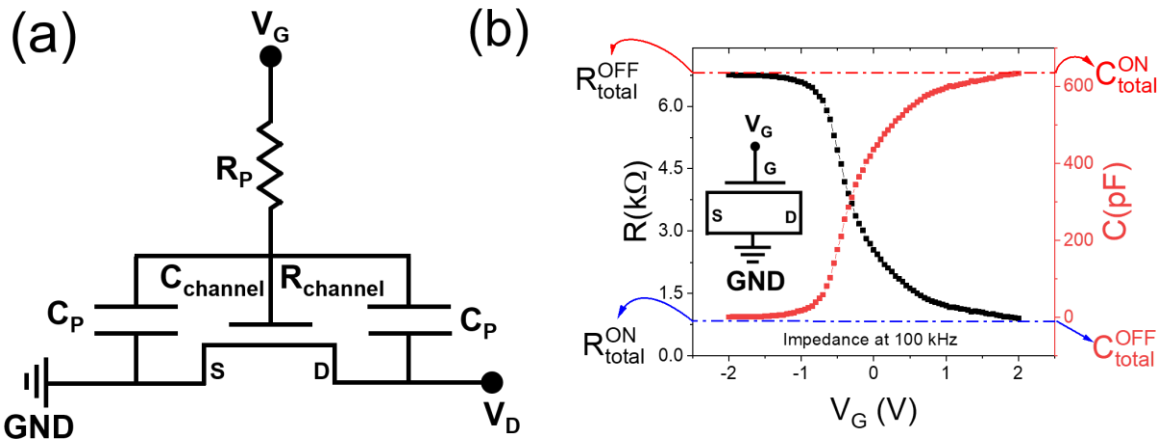

Figure 2. (A) EGT equivalent circuit highlighting parasitic resistance R_p and parasitic capacitance C_p. (B) Two terminal R-V_G and C-V_G behavior determined by impedance analysis of an EGT at 100 kHz and AC amplitude V_{AC} = 50 mV. V_G sweep rate = 100 mV/s. Inset shows the measurement configuration with V_G + V_{AC} applied to the gate, and source and drain grounded. Total two terminal resistance R_{total} and C_{total} in the fully ON and OFF states are indicated. W/L = 200 μm/10 μm.

gate (see inset in panel (b)). Figure 2b displays the R-V_G and C-V_G results at 100 kHz for a device with W/L = 200 μm/10 μm. As V_G increases, two terminal resistance drops (black curve) and capacitance increases (red curve) as the channel opens and floods with electrons. The channel is fully conducting at voltages > +1 V, and the resistance plateaus at R_{total}^{ON}= 800 Ω whereas capacitance plateaus at C_{total}^{ON} = 630 pF. For these two terminal measurements, we take R_{total}^{ON} ~

($R^{ON}_{channel}$+$R^{ON}_{contact}$)/2 + R_p. From I_D-V_G measurements, we estimate $R^{ON}_{channel}$+ $R^{ON}_{contact}$ = 10 Ω (at V_D = 0.1 V and V_G = +2 V) and therefore the entire ON-state resistance R^{ON}_{total} is effectively R_p, that is R_p ~ 800 Ω. Clearly, R_p dominates the ON-state resistance in our devices (R_p >> $R^{ON}_{channel}$ + $R^{ON}_{contact}$). On the other hand, in the case of capacitance we take $C^{ON}_{channel}$ = C^{ON}_{total} - C^{OFF}_{total} = 630 pF and C_p = C^{OFF}_{total} ~ 0 pF, i.e., C_p is below our detection limit. We thus conclude that C_p <<

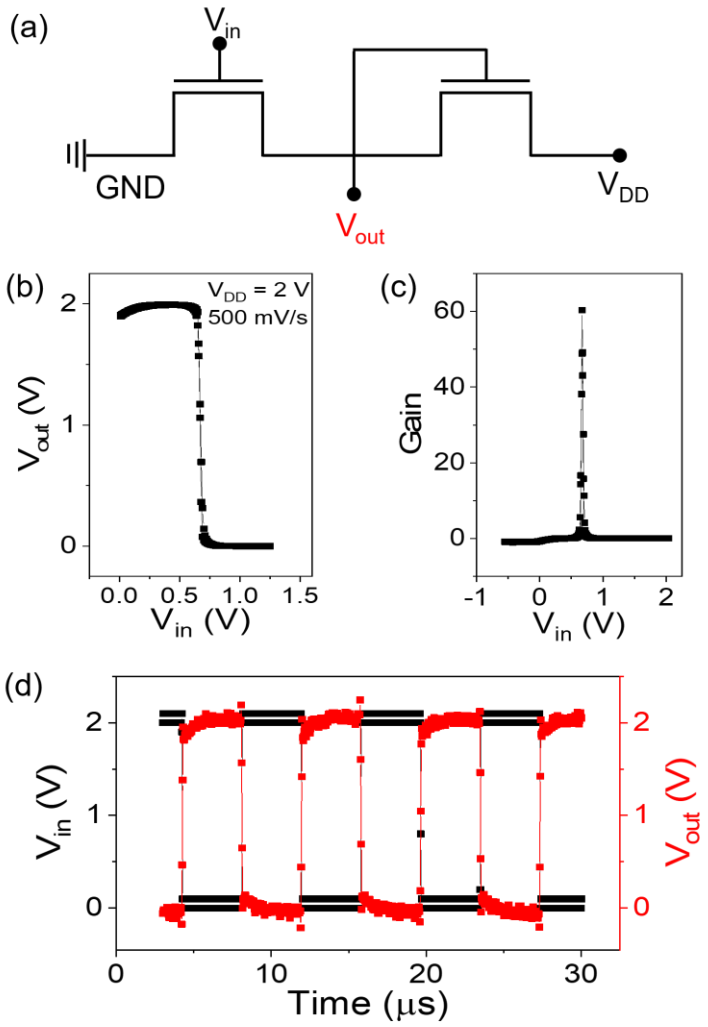

Figure 3. (A) Scheme of an inverter based on two n-channel ZnO EGTs (*W/L* = 800 μm/40 μm) in the feedback configuration in which V_{out} is connected to the gate of the load transistor. (B) Quasi-static inverter transfer characteristic with V_{DD} = +2 V and (C) the corresponding inverter gain. (D) Dynamic inverter operation at 130 kHz. The input signal is the black square wave and the output is shown in red. For this inverter, *W/L* = 600 μm/30 μm for the pair of EGTs. V_{DD} = +2 V.

$C_{channel}^{ON}$ and that C_p does not dominate the transistor response because of our efforts to minimize the electrode/electrolyte contact by insulating the source and drain electrodes. R_p, on the other hand, remains a limiting factor.

Importantly, from the values of $R_{total}^{ON} = R_p$ and $C_{total}^{ON} = C_{channel}^{ON}$ we can make an estimate of the expected switching time of our EGTs with L = 20 μm, i.e., $R_{total}^{ON} C_{total}^{ON}$ = 800 Ω x 630 x 10^{-12} F ~ 1 μs. We thus expect that these devices, even with the R_p limitation, should be capable of MHz switching, which has not been reported previously. Furthermore, decreasing the channel length L below 20 μm should lead to further decreases in switching time, as we demonstrate below.

To assess the dynamic response, we have fabricated EGT-based inverters in the internal feedback configuration in which the gate of the load EGT is connected to V_{out}, Figure 3a. A typical quasi-static inverter transfer characteristic is shown in Figure 3b and the corresponding gain (V_{out}/V_{in}) for V_{DD} = +2 V is displayed in Figure 3c. One can see in Figure 3b that a rail-to-rail voltage swing is achieved over a very small voltage interval ΔV_{in} = 50 mV. The gain is consequently 60 at V_{DD} = +2 V, a high gain for an EGT inverter, and the gain increases with increasing V_{DD} from +0.5 - +2 V as expected, Figure S4 (Supporting Information). Figure S5 demonstrates that the inverter noise margins are 0.6 V and ~80% of the theoretical maximum. Further, dynamic inverter performance at 130 kHz drive frequency is displayed in Figure 3d, where it is evident that V_{out} follows V_{in} nicely with a full rail-to-rail voltage swing.

To further quantify dynamic performance, we have fabricated five-stage ring oscillators based on six EGT inverters in which the static load transistor is tuned with a separate supply voltage V_{Bias}, Figures 4a,b. Figure 4c shows the dynamic output at V_{DD} = +3 V for a ring oscillator with 12 EGTs having channel dimensions W/L = 200/10 μm. The oscillation frequency f = 1.4

MHz. This corresponds to an average stage delay $\tau = 1/(2Nf) = 0.1/f$ = 70 ns, where N=5 is the number of stages. To our knowledge, this is the shortest propagation delay reported to date for EGT devices. To assess the impact of device scaling, we have fabricated a series of ring oscillators with systematically varying EGT channel lengths L from 10 - 40 μm and have measured dynamic

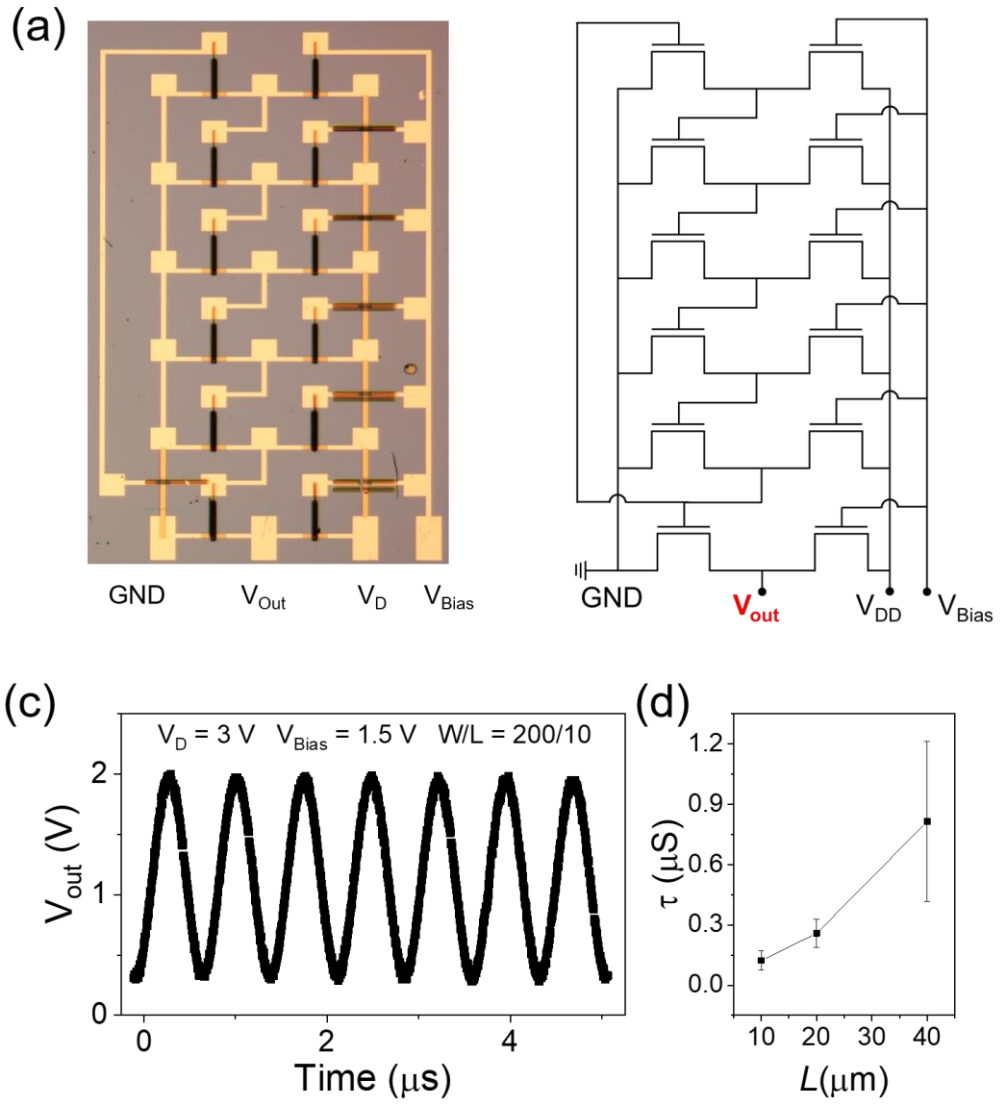

Figure 4. (A) Optical image of a five-stage ring oscillator based on EGT inverters in the static load configuration. Resistance of the load transistor is set by V_{Bias}. (B) Corresponding circuit diagram. (C) 1.4 MHz dynamic output for a five-stage oscillator at V_{DD} = +3 V and V_{Bias} = +1.5 V. EGTs have dimensions W/L = 200 μm/10 μm. (D) Propagation delay τ vs channel length L extracted from a series of ring oscillators. Channel aspect ratios W/L = 20 for each data point. Ring oscillators with L = 10 μm yielded an average τ = 120 ns. Error bars represent one standard deviation.

performance and the corresponding propagation delays. It is evident in Figure 4d that the average delay time τ is approximately 120 ns for the oscillators with the smallest (L = 10 μm) channel lengths. Furthermore, τ increases with increasing L, and for the largest devices with L = 40 μm the average τ is still less than 1 μs. There is considerably more circuit-to-circuit variability in the L = 40 μm oscillators, likely due to details associated with the fabrication process. Nevertheless, the central conclusion of Figure 4d is clear, namely that propagation delays for EGT inverters can be in the regime of 100 ns.

An increase in propagation delay τ with L is generally anticipated by analogy to conventional TFTs. Because W/L = 20, the EGT channel area $WL = 20\,L^2$. $C_{channel}^{ON}$, and therefore C_{total}^{ON}, are proportional to channel area and thus will increase as L^2. For conventional TFTs, R_{total}^{ON} does not vary with L when W/L is fixed, so the prediction would be that $\tau = R_{total}^{ON} C_{total}^{ON} \propto L^2$. However, for our EGTs the dominant role of R_p potentially introduces a different L dependence. Considering the ionic resistance between the gate and channel, one expects R_p to scale *inversely* with device area, i.e., the larger the device footprint, the smaller the ionic resistance. With this line of thought, one predicts $R_p \propto L^{-2}$ and thus the product $R_{total}^{ON} C_{total}^{ON} \propto L^{-2} \cdot L^2$ would be independent of L. That is, scaling up the device area increases C_{total}^{ON}, but decreases R_{total}^{ON} commensurately. The data in Figure 4d are clearly at odds with this simple prediction.

Here we must consider that R_p actually has two components, the ionic resistance of the gate electrolyte mentioned earlier, R_{ion}, and the resistance of the PEDOT:PSS gate electrode itself, R_{gate}, i.e., $R_p = R_{ion} + R_{gate}$. PEDOT:PSS has a far lower conductivity than typical metals (500 S/cm vs 10^5 S/cm for good metals) and thus R_{gate} can be significant. Using $R_{gate} = \rho_{pedot} \cdot 20L/(L \cdot h) = \rho_{pedot} \cdot 20/h$, where ρ_{pedot} is the PEDOT:PSS resistivity and h = 1 μm is the approximate thickness of the

ion gel, we estimate that R_{gate} = 500 – 1000 Ω for all devices. This is comparable to the resistance of the electrolyte, R_{ion}, and for the larger devices it may be the case that R_{gate} is greater than R_{ion}. Because R_{gate} is independent of *W/L* and *L*, its contribution to R_p will suppress the *L*-dependent contribution of R_{ion} and consequently the scaling of $R_{total}^{ON} = R_p = R_{ion} + R_{gate}$ for our devices may not be simple. Our empirical finding is that τ increases with *L*, broadly consistent with expectations based on C_{total}^{ON}, which dictates that larger devices should be slower. Further work is necessary to develop a quantitative model of the overall dependence of τ on device dimensions. Still, the *L*-dependence in Figure 4d suggests that there is still room to shorten EGT signal propagation delays if *L* is decreased below 10 μm and strategies are found to further diminish R_p (and contact resistance).

Conclusions

In summary, we have demonstrated here that by minimizing parasitic resistance and capacitance, and by selecting a high mobility thin film semiconductor – in this case ZnO – propagation delays for EGT inverters can be decreased into the 100 ns regime for applied biases less than 3V. For our devices, parasitic resistance remains a significant factor and further decreases in switching time will require decreases in the electrolyte, gate electrode, and source/drain contact resistances. Standardization of EGT fabrication procedures will also enhance our ability to develop quantitative models for how the EGT static *I-V* characteristics and dynamic performance scale with device dimensions. Overall, continuous improvements in EGT performance should boost ongoing efforts to employ these devices in sensors, amplifiers, neural networks, and various types of flexible, wearable devices.

Experimental Section

Materials: Ion gels were made from the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoro-methylsulfonyl)imide ([EMI][TFSI]) and the triblock copolymer poly(styrene-b-ethyl acrylate-b-styrene) (SEAS). The SEAS polymer was synthesized in-house using previously reported procedures.[43] [EMI][TFSI] ionic liquid was purchased from EMD Chemicals (Gibbstown, NJ, USA) and stored in an inert atmosphere. Aerosol jettable ion gel inks were made by preparing a solution with a mass ratio of 1:9:90 SEAS polymer:[EMI][TFSI] ionic liquid:ethyl acetate solvent. The aqueous PEDOT:PSS ink, PH1000, was purchased from Heraeus (Germany), and 6 vol% ethylene glycol was added to the ink to enhance the PEDOT conductivity on drying.

Device Fabrication: A similar fabrication process is described in prior work[30,32]. Briefly, a 50 nm thick ZnO film was deposited using atomic layer deposition (ALD) (Savannah Series, Cambridge Nano Tech) with diethylzinc and water vapor as precursors. The ZnO film was annealed in a rapid thermal annealer (RTP-600S, Modular Process Technology). The first anneal at 300 °C in N_2 lasted 15 min. The second anneal followed at 400 °C in O_2 for another 15 min. The ZnO was then patterned with standard photolithographic procedures with aqueous HCl used as an etchant.

Standard lithography processes using Shipley S1813 resist were used to make the contact pads, interconnects, and source and drain electrodes. Interconnects and contact pads were deposited in an electron beam evaporator (Temescal) with 5 nm Cr as an adhesion layer followed by 25 nm thick Au. The source and drain electrodes, which were insulated with SiOx, were made in a separate series of lithographic steps. The metal layers (60 nm Au on 10 nm Ti) were deposited via e-beam evaporation (Varian 3118). Then another photolithography process was used to deposit 10 nm Ti on top of the Au, followed by 200 nm SiOx, again by e-beam evaporation. The gate dielectric (ion gel) and gate contact (PEDOT:PSS) were sequentially printed with an aerosol jet

printer (AJ 100, Optomec) (see Figure S1). A 150 μm diameter nozzle was used to print the ion gel layers, and a 100 μm nozzle was used for PEDOT:PSS. The sheath/feed gas flow rates (in standard cm^3/min) for ion gel and PEDOT:PSS depositions were 28/8 and 17/12, respectively.

Associated Content

Supporting Information is available: Device fabrication procedure, additional device measurements.

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Notes

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